4415 72317

SEARCH REQUEST FORM Scientific and Technical Information Center - EIC2800

Rev. 8/27/01 This is an experimental format -- Please give suggestions or comments to Jeff Harrison, CP4-9C18, 306-5429.

Date 8/1/02 Serial # 09/888,957 Priority Application Date 3/17/00

Your Name M. Lewis Examiner #

AU 2822 Phone 305-3543 Room Plaza 3-3B09

In what format would you like your results? Paper is the default. PAPER DISK EMAIL

If submitting more than one search, please prioritize in order of need.

The EIC searcher normally will contact you before beginning a prior art search. If you would like to sit with a searcher for an interactive search, please notify one of the searchers.

Where have you searched so far on this case? 08-01-02

Circle: USPT DWPI EPO Abs JPO Abs 30 IN IBM TDB

Other:

What relevant art have you found so far? Please attach pertinent citations or Information Disclosure Statements.

What types of references would you like? Please checkmark:

Primary Refs ✓ Nonpatent Literature ___ Other ___

Secondary Refs ___ Foreign Patents ___

Teaching Refs ___

What is the topic, such as the **novelty**, motivation, utility, or other specific facets defining the desired **focus** of this search? Please include the concepts, synonyms, keywords, acronyms, registry numbers, definitions, structures, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract and pertinent claims.

Claims 13-21

Problem See Page 1 2nd paragraph

" " 2 last "

" " 3 1st "

Solution: novelty in structure in claims

Staff Use Only	Type of Search	Vendors
Searcher: IRINA SPECKHARD	Structure (#)	STN
Searcher Phone: 308-6559	Bibliographic ✓	Dialog ✓
Searcher Location: STIC-EIC2800, CP4-9C18	Litigation	Questel/Orbit
Date Searcher Picked Up: 8/2/02	Fulltext ✓	Lexis-Nexis
Date Completed: 8/2/02	Patent Family	WWW/Internet
Searcher Prep/Rev Time: 110	Other	Other
Online Time: 120		

8/2/02

Examiner Lewis,

AU 2822
CP3-3B07

Re: 09/808,957

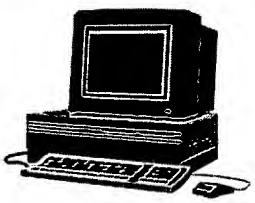
Please find attached edited first-pass search results from the patent and non-patent commercial abstract and full-text databases. The search strategy was based on the claims and the statements of the technical problems and solutions. Tagged records might be worth your review as well as the rest of the references provided.

If you have any further questions, please let me know.

Thank You,

Irina Speckhard
308-6559
STIC-EIC2800
CP4-9C18

EIC2800
Search Results
Feedback Form (Optional)



Scientific & Technical Information Center

The search results generated for your recent request are attached. If you have any questions or comments (compliments or complaints) about the scope or the results of the search, please contact ***the EIC searcher*** who conducted the search ***or contact***:

Jeff Harrison, Team Leader, 306-5429

Voluntary Results Feedback Form

- *I am an examiner in Workgroup:* ☐ *Example:* 2830

- *Relevant prior art **found**, search results used as follows:*
  - ☐ 102 rejection
  - ☐ 103 rejection
  - ☐ Cited as being of interest.
  - ☐ Helped examiner better understand the invention.
  - ☐ Helped examiner better understand the state of the art in their technology.

Types of relevant prior art found:

- ☐ Foreign Patent(s)
- ☐ Non-Patent Literature
  (journal articles, conference proceedings, new product announcements etc.)

- *Relevant prior art **not found***:
  - ☐ Results verified the lack of relevant prior art (helped determine patentability).
  - ☐ Search results were not useful in determining patentability or understanding the invention.

Other Comments:

Drop off completed forms in **CP4-9C18,** or send to **Jeff Harrison, CP4-9C18.**

08/02/2002 09/808,957

02aug02 10:33:32 User267149 Session D258.2

File 350:Derwent WPIX 1963-2002/UD,UM &UP=200249
(c) 2002 Thomson Derwent
*File 350: Alerts can now have images sent vial all delivery methods.
See HELP ALERT and HELP PRINT for more info.
? E PN=JP 2000075755
? S E3
? MAP PN/CT=
Serial#SD110

CITATION SEARCH - NO RESULTS

? MAP PN/CG=

Serial#SD111
02aug02 10:34:30 User267149 Session D258.3

File 342:Derwent Patents Citation Indx 1978-01/200209C
(c) 2002 Thomson Derwent
*File 342: Updates 200160-200209 replaced. See HELP NEWS 342.
Alert feature enhanced for multiple files, etc. See HELP ALERT.

? EXS SD110
S1 0 CT=JP 2000075755
? EXS SD111
S2 0 CG=JP 2000075755
? B 350,347

SYSTEM:OS - DIALOG OneSearch
File 350:Derwent WPIX 1963-2002/UD,UM &UP=200249
(c) 2002 Thomson Derwent
*File 350: Alerts can now have images sent vial all delivery methods.
See HELP ALERT and HELP PRINT for more info.
File 347:JAPIO Oct 1976-2002/Mar(Updated 020702)
(c) 2002 JPO & JAPIO
*File 347: JAPIO data problems with year 2000 records are now fixed.
Alerts have been run. See HELP NEWS 347 for details.

? EXS SD110
S1 0 CT=JP 2000075755
? EXS SD111
S2 0 CG=JP 2000075755

08/02/2002 09/808,957 [redacted]

02aug02 10:53:03 User267149 Session D259.1

SYSTEM:OS - DIALOG OneSearch
File 2:INSPEC 1969-2002/Jul W4
(c) 2002 Institution of Electrical Engineers
*File 2: Alert feature enhanced for multiple files, duplicates removal, customized scheduling. See HELP ALERT.
File 6:NTIS 1964-2002/Aug W2
(c) 2002 NTIS, Intl Cpyrght All Rights Res
*File 6: Alert feature enhanced for multiple files, duplicates removal, customized scheduling. See HELP ALERT.
File 8:Ei Compendex(R) 1970-2002/Jul W4
(c) 2002 Engineering Info. Inc.
*File 8: Alert feature enhanced for multiple files, duplicates removal, customized scheduling. See HELP ALERT.
File 34:SciSearch(R) Cited Ref Sci 1990-2002/Aug W1
(c) 2002 Inst for Sci Info
*File 34: Alert feature enhanced for multiple files, duplicates removal, customized scheduling. See HELP ALERT.
File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
(c) 1998 Inst for Sci Info
File 35:Dissertation Abs Online 1861-2002/Jun
(c) 2002 ProQuest Info&Learning
File 65:Inside Conferences 1993-2002/Jul W4
(c) 2002 BLDSC all rts. reserv.
File 77:Conference Papers Index 1973-2002/Jul
(c) 2002 Cambridge Sci Abs
File 94:JICST-EPlus 1985-2002/Jun W1
(c)2002 Japan Science and Tech Corp(JST)
*File 94: There is no data missing. UDs have been adjusted to reflect the current months data. See Help News94 for details.
File 99:Wilson Appl. Sci & Tech Abs 1983-2002/Jun
(c) 2002 The HW Wilson Co.
File 108:Aerospace Database 1962-2002/Jul
(c) 2002 AIAA
File 144:Pascal 1973-2002/Jul W4
(c) 2002 INIST/CNRS
File 238:Abs. in New Tech & Eng. 1981-2002/Jul
(c) 2002 Reed-Elsevier (UK) Ltd.
File 305:Analytical Abstracts 1980-2002/Jul W3
(c) 2002 Royal Soc Chemistry
*File 305: Alert feature enhanced for multiple files, duplicate removal, customized scheduling. See HELP ALERT.
File 315:ChemEng & Biotec Abs 1970-2002/Jun
(c) 2002 DECHEMA
File 350:Derwent WPIX 1963-2002/UD,UM &UP=200249
(c) 2002 Thomson Derwent
*File 350: Alerts can now have images sent vial all delivery methods. See HELP ALERT and HELP PRINT for more info.
File 344:Chinese Patents Abs JuL 1985-2002/JuL
(c) 2002 European Patent Office
File 347:JAPIO Oct 1976-2002/Mar(Updated 020702)
(c) 2002 JPO & JAPIO
*File 347: JAPIO data problems with year 2000 records are now fixed.

STIC-EIC 2800 CP4-9C18 Irina Speckhard 308-6559

08/02/2002 09/808,957

Alerts have been run. See HELP NEWS 347 for details.
File 371:French Patents 1961-2002/BOPI 200209

STIC-EIC 2800 CP4-9C18 Irina Speckhard 308-6559

09/808,957

08/02/2002 [redacted]

Set	Items	Description
S1	40215	(THIN()FILM()TRANSISTOR) OR TFT
S2	3328	MC=U11-C18A1
S3	40993	S1:S2
S4	172641	LCD OR (LIQUID()CRYSTAL()DISPLAY? ?)
S5	19184	MC=(U14-K01A1J OR U14-K01 OR U14-H01A OR U14-K01A2B)
S6	253554	IC=(H01L-029 OR G02F-001/13)
S7	402436	S4:S6
S8	17774	MANUFACT??????(3N)SUBSTRATE? ?
S9	44	(MANUFACT??????(3N)SUBSTRATE? ?)(3N)(INORGANIC?????? OR ARTIFICIAL? ? OR SYNTHETIC??????)
S10	81	MANUFACT??????(3N)SUBSTRATE? ?(3N)(INORGANIC?????? OR ARTIFICIAL? ? OR SYNTHETIC??????)
S11	81	S9:S10
S12	2999269	(INORGANIC?????? OR ARTIFICIAL? ? OR SYNTHETIC??????)
S13	2999269	S9:S12
S14	9467	PRODUCT? ?(3N)SUBSTRATE? ?
S15	44	PRODUCT? ?(3N)(SUBSTRATE(3N)ORGANIC??????)
S16	3323729	ORGANIC??????
S17	3323729	S15:S16
S18	1712	(BOND?????? OR JOIN??????)()SUBSTRATE? ?
S19	5547	MOISTUR??????(3N)PROOF
S20	16647	MOISTUR??????(3N)(LAYER??? OR FILM??? OR COAT??? OR MULTILAYER??? OR SPACER???)
S21	11159	PIXEL? ?(3N)(ELECTRODE? ? OR MICROELECTRODE? ? OR CONDUCT?????)
S22	4086426	ELECTRODE? ? OR MICROELECTRODE? ? OR CONDUCT????
S23	282166	(CONDUCT??????)(3N)(LAYER??? OR FILM??? OR COAT??? OR MULTILAYER??? OR SPACER???)
S24	12043	CC=(B2110 OR B2160 OR B8130)
S25	4739	MC=(S05-A02 OR S05-D01A1A OR U11-C05C4)
S26	7692	IC=(A61N-001/04 OR A61N-001/06 OR A61B-005/04)
S27	4670	MC=(V05-D07C5C OR V07-F01A1)
S28	107520	IC=(H01J-029/89 OR G02B-006)
S29	4224858	S22:S28
S30	9043	(ELECTRO()LUMINESCEN?????? OR ELECTROLUMINESCEN??????)(3N)(DISPLAY?????? OR SCREEN? ?)
S31	20746	S19:S20
S32	28635	S3 AND S7
S33	3	S32 AND S11
S34	3	RD (unique items)
S35	28632	S32 NOT S34
S36	558	S35 AND S8
S37	9	S36 AND S13
S38	9	RD (unique items)
S39	9	IDPAT (sorted in duplicate/non-duplicate order)
S40	9	IDPAT (primary/non-duplicate records only)
S41	549	S36 NOT S40
S42	3	S41 AND S14
S43	546	S41 NOT S42
S44	18	S43 AND S17
S45	18	RD (unique items)
S46	18	IDPAT (sorted in duplicate/non-duplicate order)

S47	18	IDPAT (primary/non-duplicate records only)
S48	528	S43 NOT S47
S49	0	S48 AND S18
S50	0	S48 AND S31
S51	105	S48 AND S21
S52	105	S51 AND S29
S53	0	S52 AND S30
S54	105	S52 AND S8
S55	0	S52 AND S12
S56	0	S52 AND S17
S57	105	S52 AND S7
S58	3118	S7 AND S8
S59	91	S58 AND S13
S60	5	S59 AND S21
S61	86	S59 NOT S60
S62	1	S61 AND S18
S63	85	S61 NOT S62
S64	22	S63 AND S17
S65	1	S64 AND S31
S66	21	S64 NOT S65
S67	11	S66 AND S29
S68	11	RD (unique items)
S69	11	S68 NOT S42,S47
S70	74	S63 NOT S69
S71	23	S3 AND S31
S72	0	S71 AND S8
S73	1	S71 AND S13
S74	22	S71 NOT S73
S75	5	S74 AND S17
S76	5	RD (unique items)
S77	17	S74 NOT S76
S78	0	S77 AND S14
S79	7	S77 AND S29
S80	7	RD (unique items)

34/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014333271
WPI Acc No: 2002-153974/200220
XRPX Acc No: N02-117090
Thin film semiconductor device manufacturing method for **liquid crystal display**, involves bonding manufacturing substrate to rear of product substrate and forming **thin film transistor** on product substrate
Patent Assignee: SONY CORP (SONY)
Inventor: HAYASHI H
Number of Countries: 003 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20010022362	A1	20010920	US 2001808957	A	20010316	200220	B
JP 2001267578	A	20010928	JP 200075755	A	20000317	200220	
KR 2001091992	A	20011023	KR 200112703	A	20010312	200222	

Priority Applications (No Type Date): JP 200075755 A 20000317
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20010022362	A1		10	H01L-031/36	
JP 2001267578	A		8	H01L-029/786	
KR 2001091992	A			H01L-029/786	

Abstract (Basic): US 20010022362 A1
Abstract (Basic):
NOVELTY - A **thin film transistor** is formed on organic product **substrate** (1) after bonding an **inorganic manufacturing substrate** (20) to back side, for supporting the product substrate. After transistor formation, the manufacturing substrate is separated from the product substrate.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:
(a) **Liquid crystal display** device manufacturing method;
(b) Electroluminescence display device manufacturing method;
(c) Thin film semiconductor device;
(d) **Liquid crystal display** device;
(e) Electroluminescence display device
USE - For electroluminescence **liquid crystal display** device (claimed) used in portable electronic equipments such as palm-top computers or portable telephones.
ADVANTAGE - Since the **thin film transistor** is integrated and formed on the substrate reinforced with bonding, the manufacturing process is stabilized. Since the manufacturing substrate after use is separated and the product is completed, the product itself is reduced in weight and thickness. The separated manufacturing substrate is further utilized again to the **thin film transistor** manufacturing process, making it possible for recycling of resource. By using energy such as supersonic waves or

laser beams, the dissolution of the adhesives is promoted.

DESCRIPTION OF DRAWING(S) - The figure shows the thin film semiconductor device during manufacture.

Substrates (1,20)

08/02/2002 [redacted]

34/3,AB/2 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

04488402
METHOD OF MANUFACTURE **THIN FILM TRANSISTOR**

PUB. NO.: 06-132302 [JP 6132302 A]
PUBLISHED: May 13, 1994 (19940513)
INVENTOR(s): SHIMANO TAKUYA
IBARAKI NOBUKI
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 04-282099 [JP 92282099]
FILED: October 21, 1992 (19921021)
JOURNAL: Section: E, Section No. 1589, Vol. 18, No. 419, Pg. 146, August 05, 1994 (19940805)

ABSTRACT

PURPOSE: To enable the high operational characteristics to be displayed by a method wherein an amorphous silicon thin film ions are implanted using an inorganic protective film as an implantation stopper to form low resistance semiconductor layers and then at least either one out of the film thickness or the outside dimension of the inorganic protective film is to be reduced.
CONSTITUTION: The **thin film transistor** composed of a gate electrode 12, a gate insulating film 13, an amorphous silicon thin film, low resistance semiconductor layers 18a, 18b, an inorganic protective film 15, a source electrode 19 and a drain electrode 20 formed on an insulating **substrate** 11 is **manufactured**. At this time, the **inorganic** protective film 15 is formed into a shape on the amorphous silicon thin film to implant ion species containing impurity element ions in the amorphous silicon thin film using the inorganic protective film 15 as an implantation stopper for the formation of the low resistance semiconductor layers 18a, 18b. Later, at least either one out of the film thickness or the outside dimension of the inorganic protective film 15 is reduced. For example, the inorganic protective film 15 is etched away using a hydrofluoric acid base processing solution to remove a part of an ion implanting part 17a.

34/3,AB/3 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

02641173
THIN-FILM TRANSISTOR

PUB. NO.: 63-258073 [JP 63258073 A]
PUBLISHED: October 25, 1988 (19881025)
INVENTOR(s): MIYASAKA TSUGUMITSU
APPLICANT(s): SEIKO EPSON CORP [000236] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 62-092425 [JP 8792425]
FILED: April 15, 1987 (19870415)
JOURNAL: Section: E, Section No. 718, Vol. 13, No. 78, Pg. 37, February 22, 1989 (19890222)

ABSTRACT

PURPOSE: To protect a substrate from deformation in a heat treatment at 1000-1150 deg.C and **TFT** characteristics from changes during operation at 100 deg.C or higher by a method wherein an Si film is formed on a quartz glass substrate containing a specified quantity of Al after synthesis by a sol.gel method and the upper layer thereof is subjected to a thermal oxidation process for the formation of a gate insulating film.

CONSTITUTION: A **synthetic** quartz glass **substrate** is **manufactured** by a sol.gel method and contains Al whose quantity is somewhere in a 3-150ppm range. A silicon film is formed on the substrate and the upper layer of the silicon film is thermally oxidized for the formation of a gate insulating film of silicon dioxide. A prescribed quantity of Al is allowed by using the sol.gel method to be in the high-purity synthetic quartz substrate. The presence of the Al in the quartz improves on the heat-resisting feature of the quartz without changes in its characteristics. Such a substrate is protected from deformation at 1000-1150 deg.C in a **TFT** manufacturing process and a **TFT** constructed on the substrate is protected from changes in its characteristics during operation even if its temperature rises as high as 230 deg.C.

40/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014567416
WPI Acc No: 2002-388119/200242
XRAM Acc No: C02-109729
XRPX Acc No: N02-304153
Manufacture of ammonium cerium (IV) nitrate used as oxidizing agent or catalyst for synthesis of organic compound, involves adding ammonium nitrate to aqueous solution of nitric acid and cerium hydroxide
Patent Assignee: ASAHI KAGAKU KOGYO KK (ASAH)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2002068741	A	20020308	JP 2000254345	A	20000824	200242	B

Priority Applications (No Type Date): JP 2000254345 A 20000824
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2002068741	A		6	C01F-017/00	

Abstract (Basic): JP 2002068741 A
Abstract (Basic):
NOVELTY - The cerium hydroxide containing tetravalent cerium and trivalent cerium is dissolved in 50 weight% (wt.%) or more of aqueous solution of nitric acid. The ratio of tetravalent cerium to total cerium in cerium hydroxide, is 80% or more. Subsequently, ammonium nitrate is added, to precipitate crystal of ammonium cerium (IV) nitrate. The precipitated crystal of ammonium cerium (IV) nitrate is then separated.
DETAILED DESCRIPTION - The cerium hydroxide containing tetravalent cerium and trivalent cerium is dissolved in 50 weight% (wt.%) or more of aqueous solution of nitric acid such that the molar ratio of nitric acid with respect to cerium is 4 or more. The ratio of tetravalent cerium to total cerium in cerium hydroxide, is 80% or more. Subsequently, ammonium nitrate is added such that the molar ratio of ammonium nitrate with respect to cerium is 1.5 or more to precipitate crystal of ammonium cerium (IV) nitrate. The precipitated crystal of ammonium cerium (IV) nitrate is then separated. An INDEPENDENT CLAIM is included for etching agent for etching chromium thin film used in liquid crystal **substrate manufacturing** process. The etching agent contains aqueous solution of ammonium cerium (IV) nitrate and perchloric acid or nitric acid.
USE - For manufacturing ammonium cerium (IV) nitrate used as oxidizing agent or catalyst for synthesis of organic compound, or as etching agent for etching chromium thin film (claimed) used during production of color filter and **TFT** array of **liquid crystal display** panel.
ADVANTAGE - Ammonium cerium (IV) nitrate of high purity is produced in high yield, in short period of time.
pp; 6 DwgNo 0/0

40/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014565302
WPI Acc No: 2002-386005/200242
XRAM Acc No: C02-108795
XRPX Acc No: N02-302253
Developer for photosensitive resin image development, consists of amine compound having preset pH and pKa, as developing component
Patent Assignee: FUJI PHOTO FILM CO LTD (FUJF)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2001228628	A	20010824	JP 200038663	A	20000216	200242	B

Priority Applications (No Type Date): JP 200038663 A 20000216
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2001228628	A		16	G03F-007/32	

Abstract (Basic): JP 2001228628 A
Abstract (Basic):
NOVELTY - A developer contains amine compound as developing agent. The pH value and pKa value of amine compound satisfies preset relation.
DETAILED DESCRIPTION - A developer contains amine compound as developing agent. The pH value and pKa value of amine compound satisfies the relation (amine compound pKa-0.5)at mostpHat most(amine compound pKa+1.2). INDEPENDENT CLAIMS are also included for the following: (i) Image formation method which involves forming a photosensitive layer containing photosensitive resin for alkali image development, on a substrate. The photosensitive layer is subjected to pattern exposure and image is developed using the developer; (ii) Manufacture of color filter which involves forming image on substrate using the developer. The photosensitive layer further includes a coloring agent; (iii) **Manufacture** of active matrix **substrate** with a color filter. A photosensitive layer which consists of photosensitive resin and coloring agent, is formed on an active matrix substrate. A pattern exposure is carried out and the colored image is formed on the substrate; and (iv) **Liquid crystal display** element comprising liquid crystal material sealed in between active matrix substrate with the color filter and opposing transparent substrate.
USE - For photosensitive resin image development used in manufacture of color filter, active matrix substrate with color filter for **liquid crystal display** element (claimed). Also as display board using flat surface display for production of printed circuit boards, portable information terminal, personal computer, word processor and amusement devices.
ADVANTAGE - The developer has excellent time dependent stability which forms a high definition image stably. Developing property reduction by pH change is avoided during developing. A colored image of high resolution can be formed on active matrix substrate without

causing bad influence to semiconductor characteristics of **thin film transistor** element. **Liquid crystal display** element of high resolution and pattern accuracy can be provided, inexpensively.

08/02/2002 [redacted]

40/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014534719
WPI Acc No: 2002-355422/200239
XRAM Acc No: C02-101086
XRPX Acc No: N02-279410
Polycrystalline thin film manufacture, for manufacture of semiconductor, involves heat-processing substrate with sequentially formed amorphous and metal films, and light and heat annealing formed polycrystalline film
Patent Assignee: TOYOTA CHUO KENKYUSHO KK (TOYW)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2002008977	A	20020111	JP 2000187175	A	20000622	200239	B

Priority Applications (No Type Date): JP 2000187175 A 20000622
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2002008977	A		9	H01L-021/20	

Abstract (Basic): JP 2002008977 A
Abstract (Basic):
NOVELTY - The manufacture of a polycrystalline thin film involves forming sequentially an amorphous silicon film (31) and a metal film (31), on a quartz substrate (35). The substrate is heat-processed to form polycrystalline thin film (36). A portion or all of the metal film is removed and the substrate is irradiated with light, and the polycrystalline film is modified by laser and heat annealing.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for the manufacture of a semiconductor device.
USE - For the manufacture of a polycrystalline silicon film on **substrate** for the **manufacture** of a semiconductor device (claimed), such as a **thin film transistor**.
ADVANTAGE - A polycrystalline thin film of good quality is produced. A semiconductor device with reduced leakage electric current and contact resistance is manufactured.
DESCRIPTION OF DRAWING(S) - The figure shows the manufacture of the semiconductor device.
Amorphous silicon film (31)
Quartz substrate (35)
Polycrystalline thin film (36)
pp; 9 DwgNo 2/5

40/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014208215
WPI Acc No: 2002-028912/200204
XRAM Acc No: C02-008166
XRPX Acc No: N02-022404
Manufacture of microlens **substrate** used in liquid crystal panels, involves hardening a resin placed in concave cavity of a substrate
Patent Assignee: SEIKO EPSON CORP (SHIH)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2001141907	A	20010525	JP 99323165	A	19991112	200204	B

Priority Applications (No Type Date): JP 99323165 A 19991112
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2001141907	A		15	G02B-003/00	

Abstract (Basic): JP 2001141907 A
Abstract (Basic):
NOVELTY - A resin layer (9) is provided on a substrate (2) with several concave portions (3). Another substrate (8) is then placed on the resin layer and the resin is hardened to form microlens (4) in the concave portions. The resin had a rate of shrinkage of 8.8% or less before hardening.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following: (i) Microlens substrate (1); (ii) Opposing substrate (10) for liquid crystal panels (16) which has a transparent electrically conductive film (12) provided on substrate (2) or (8); (iii) Liquid crystal panel; and (iv) Projection type display device which has a light valve through which an image is projected.
USE - For opposing substrates of liquid crystal panels and projection type display devices (all claimed).
ADVANTAGE - The microlens substrate has high ultraviolet rays resistance. Generation of defects, air bubbles, peeling and cloudiness are prevented.
DESCRIPTION OF DRAWING(S) - The figure shows the cross-sectional view of liquid crystal panel.
Microlens substrate (1)
Substrates (2,8)
Concave portion (3)
Microlens (4)
Resin layer (9)
Opposing substrate (10)
Black matrix (11)
Transparent film (12)
Liquid crystal panel (16)
TFT substrate (17)
Pixel electrode (172)
Thin film transistor (173)

40/3,AB/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013796410
WPI Acc No: 2001-280621/200129
XRAM Acc No: C01-085087
XRPX Acc No: N01-200035

Manufacturing **liquid crystal display**, by forming light developable organic layer over substrate surface, and removing residual portion of light developable organic layer remaining on drain electrode and data pad

Patent Assignee: LG LCD INC (GLDS)
Inventor: KIM J H; KIM W K; PARK J Y

Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6204081	B1	20010320	US 99315650	A	19990520	200129	B

Priority Applications (No Type Date): US 99315650 A 19990520
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6204081	B1		12	H01L-021/00	

Abstract (Basic): US 6204081 B1
Abstract (Basic):

NOVELTY - A **liquid crystal display** (**LCD**) is manufactured by forming a light developable organic layer over substrate surface on which **thin film transistor** is formed, and removing a residual portion of the light developable organic layer remaining on surface of drain electrode and data pad and exposing surface of gate pad.

DETAILED DESCRIPTION - Manufacturing an **LCD** comprises forming a **thin film transistor** over a substrate, forming a light developable organic layer over an entire surface of the substrate, partially exposing a part of drain electrode, data pad, and gate insulating layer over a gate pad, and forming a transparent conductive layer in contact with the exposed drain electrode, data pad, and gate pad and which covers a part of the surface of the etched light developable organic layer. The **thin film transistor** comprises the drain electrode (170d), data pad (170c) and data insulating layer over the gate pad (160b).

USE - For manufacturing **LCD**.

ADVANTAGE - By using the light developable BCB protection layer, there is no need to apply a photoresist in order to pattern the light protection layer. The occurrence of the jagged protruding portion or other developable protection later caused by an error in the thickness of the applied photoresist is prevented thus the manufacturing of the **LCD** is simplified compared to conventional method. The pixel electrodes can be patterned accurately and defective patterning of the pinhole of the pixel electrode is prevented.

DESCRIPTION OF DRAWING(S) - The figure is a cross-sectional views illustrating **manufacturing** steps of a **substrate**.

40/3,AB/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013503387
WPI Acc No: 2000-675328/200066
XRAM Acc No: C00-205081
XRPX Acc No: N00-500682
Cleaning of **substrate** used for **manufacture** of electron source **substrate**, involves using cleaning liquid containing chelating reagent, capable of forming insoluble chelate compound with metal ion on substrate
Patent Assignee: CANON KK (CANO)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2000251799	A	20000914	JP 9951221	A	19990226	200066	B

Priority Applications (No Type Date): JP 9951221 A 19990226
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2000251799	A		10	H01J-031/12	

Abstract (Basic): JP 2000251799 A
Abstract (Basic):

NOVELTY - An aqueous cleaning liquid is contacted with a substrate surface used for electronic element formation to elute metal ion adhered on substrate. The cleaning liquid contains a chelating agent capable of forming an insoluble chelate compound with metal ion, in water. The insoluble chelate compound formed after cleaning is then removed.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following: (i) manufacture of electron source board (31). A conductive film having electron emission portion on an insulated substrate is provided between a pair of element electrodes. The wirings crossing the insulated film are mutually insulated. One of the element electrode are connected to wiring along lengthwise direction and other is connected to wiring along crosswise direction; and (ii) image forming apparatus comprising electron source board provided with electron emitting elements and light emission display board. The source and display board are positioned opposite to each other.

USE - For cleaning substrate used for forming functional substrates such as electron source board used in image forming apparatus, **liquid crystal display** device, **thin film transistor/liquid crystal display** device, plasma display, low speed electron beam fluorescent display tube and cathode ray tube.

ADVANTAGE - Foreign materials such as metal ions (especially lead ions) adhered on the substrate surface can be effectively washed. The image forming apparatus using the functional substrate forms high resolution image.

DESCRIPTION OF DRAWING(S) - The figure shows substrate cleaning method.

40/3,AB/7 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012443465
WPI Acc No: 1999-249573/199921
XRPX Acc No: N99-186185
TFT substrate manufacturing method for **LCD** device used in TV - involves forming source-drain electrodes on pixel electrode using photoresist as mask
Patent Assignee: MATSUSHITA DENKI SANGYO KK (MATU)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 11072802	A	19990316	JP 97235163	A	19970829	199921	B

Priority Applications (No Type Date): JP 97235163 A 19970829
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 11072802	A		6	G02F-001/136	

Abstract (Basic): JP 11072802 A

NOVELTY - The photosensitive resist is coated on the pixel electrode material (5) and exposure and development is carried out. The source-drain electrodes are formed on the pixel electrode material and connected to TFTs through the contact holes (4a). DETAILED DESCRIPTION - The drive TFTs are formed on a substrate (1). The insulation film (4) is coated on the substrate by exposing it to the adhesion reinforcement agent (10). The contact holes (4a) are formed in the insulation film by executing exposure and development on it using the photomask with specific pattern. The pixel electrode material (5) is formed on the insulating film. **INORGANIC** CHEMISTRY - The drain electrode is formed by material selected from group of iron, cobalt, nickel, chromium, titanium, molybdenum.

USE - For **LCD** device used in OA apparatus, TV, image display device, information terminal.

ADVANTAGE - Improves yield of **TFT** array substrate by increasing adhesion of wiring and **TFT**. Improves reliability of **TFT** array substrate. DESCRIPTION OF DRAWING(S) - The figure shows sectional view showing structure of **TFT** array substrate. (1) Substrate; (4) Insulation film; (4a) Contact holes; (5) Pixel electrode; (10) Adhesion reinforcement agent.

40/3,AB/8 (Item 8 from file: 347)
DIALOG(R)File 347:JAPIO

06883203
ELIMINATING METHOD OF ORGANIC THIN FILM, MANUFACTURING METHOD OF SEMICONDUCTOR DEVICE AND **LIQUID CRYSTAL DISPLAY** DEVICE USING THE METHOD, AND ELIMINATING EQUIPMENT OF ORGANIC THIN FILM USED FOR MANUFACTURING

PUB. NO.: 2001-110711 [JP 2001110711 A]
PUBLISHED: April 20, 2001 (20010420)
INVENTOR(s): OGAWA KAZUFUMI
APPLICANT(s): MATSUSHITA ELECTRIC IND CO LTD
APPL. NO.: 11-289580 [JP 99289580]
FILED: October 12, 1999 (19991012)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a method to perfectly eliminate an organic coating film by oxidation at a comparatively low temperature without damaging device characteristic when manufacturing a **TFT** array and a semiconductor device, and excludes contaminating factor to a device.

SOLUTION: In this method, at least an organic coating film formed on an **inorganic** substrate is eliminated by oxidation in supercritical water. At this time, silicon for manufacturing a semiconductor element, a glass **substrate** for **manufacturing** a **liquid crystal display** element, etc., are assumed as the **inorganic** substrate. It is effective in a resist eliminating process that resist for lithography is assumed as the organic coating film.

40/3,AB/9 (Item 9 from file: 347)
DIALOG(R)File 347:JAPIO

05748127
THIN FILM TRANSISTOR ARRAY **SUBSTRATE** AND ITS **MANUFACTURE**

PUB. NO.: 10-031227 [JP 10031227 A]
PUBLISHED: February 03, 1998 (19980203)
INVENTOR(s): MAEDA AKIYOSHI
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 08-184325 [JP 96184325]
FILED: July 15, 1996 (19960715)

ABSTRACT

PROBLEM TO BE SOLVED: To prevent corrosion and to make it possible to secure connection reliability in a connection terminal part by coating a high melting point metallic film arranged in a contact hole inner wall peripheral parts constituting respective connection terminal parts in a buried shape with a gate insulation film and an **inorganic** insulating film.

SOLUTION: A source electrode 22, a drain electrode 23, a pixel electrode part 15, a signal line and respective connecting terminal parts between scan lines and the signal lines are constituted containing at least the same transparent conductive film 34 as a conductive member. Further, in respective connection terminal parts, the conductive member 34 is constituted so as to be exposed through the contact hole provided on a proper insulation film 33. Then, a high melting point metallic film layer 35 is exposed and arranged on a boundary part between the conductive member 34 and the contact hole inner wall party provided on the insulation film 33 in respective connection terminal parts. Further, the contact hole inner wall part that at least the high melting point metallic film layer 35 is exposed is coated with the **inorganic** insulation film 38.

42/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010161245
WPI Acc No: 1995-062498/199509
XRAM Acc No: C95-027696
XRPX Acc No: N95-049762
Colour filter mfg. process, used for coloured **liquid crystal display** or matrix type colour display having **thin film transistor** - includes forming window-shaped, coloured coating films over electrically conductive circuits and a surrounding black matrix frame of functional coating film on a transparent substrate
Patent Assignee: SHINTO PAINT CO LTD (SHID); SUMITOMO CHEM CO LTD (SUMO)
Inventor: MATSUMURA M; MIYAZAKI S; NAKANO T; OKADA Y; TESHIMA Y
Number of Countries: 011 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 636932	A1	19950201	EP 94111562	A	19940725	199509	B
FI 9403497	A	19950127	FI 943497	A	19940725	199516	
US 5503732	A	19960402	US 94273967	A	19940712	199619	
TW 318260	A	19971021	TW 94106791	A	19940725	199808	
KR 305443	B	20011122	KR 9418047	A	19940726	200244	

Priority Applications (No Type Date): JP 93183796 A 19930726
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 636932	A1	E	10	G03C-007/12	
Designated States (Regional): CH DE FR GB LI NL SE					
FI 9403497	A			H01L-000/00	
US 5503732	A		7	C25D-007/00	
TW 318260	A			H01L-021/027	
KR 305443	B			G02F-001/1335	Previous Publ. patent KR 95003895

Abstract (Basic): EP 636932 A
Transparent substrate (1) having electrically conductive circuits (2) on its surface is coated with a negative or positive photoresist compsn. forming a functional coating film (3) which is pattern-exposed to light using a photomask and developed leaving a frame-shaped coating film defining uncovered window-shaped areas (4) over the circuits. The resulting substrate is subjected to electro-deposition using the circuits on the substrate as one electrode so as to form coating films (7,8,9) over the window-shaped areas. Also claimed is the resulting substrate having electrically conductive circuits on its surface covered by window-shaped coating films and frame-shaped, functional coating films at regions not occupied by the window-shaped coating films.
USE - Method is used to produce a colour filter used in a colour **liquid crystal display** or a matrix type colour display formed using a **thin film transistor**.
ADVANTAGE - Method enables coating films to be formed with high precision.
Dwg.1/2
Abstract (Equivalent): US 5503732 A

A method for **manufacturing** a **substrate** having electrically conductive circuits on the surface of it, window-shaped coloured coating films on the circuits and a frame-shaped, light-screening coating film at the regions not occupied with the window-shaped coating films, which comprises the steps of: (a) coating a transparent substrate having more than one transparent, electrically conductive circuit on the surface of it with a negative or positive photoresist composition capable of giving a light-screening coating film to cover the circuits-carrying surface of the substrate, followed by forming a light-screening coating film, (b) superposing, on the surface of the coating film formed through step (a), a photomask having a pattern designed so as to give in the following step (c) the coating film covering the frame-shaped part and uncovering the window-shaped parts, and exposing the thus masked coating film to light, (c) subjecting the resulting substrate formed through steps (a) and (b) to development, leaving the frame-shaped light-screening coating film and eliminating the coating film other than the frame-shaped light-screening coating film, (d) subjecting the resulting substrate formed through steps (a), (b) and (c) in this order to electro-deposition selecting less than all the circuits on the substrate as one electrode, forming at least one electro-deposition coloured coating film at the window-shaped parts on the circuits, and (e) recovering a **product** comprising a transparent **substrate** having more than one transparent circuit on it, frame-shaped light-screening coating film defining windows and at least one coloured coating film within the windows.

42/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008830168
WPI Acc No: 1991-334184/199146
XRAM Acc No: C91-144186
XRPX Acc No: N91-256092
Prepn. of semi-crystalline semiconductor thin film transistors - for use as drivers for image displacing devices produced at reduced manufacturing cost
Patent Assignee: ASAHI GLASS CO LTD (ASAG)
Inventor: MASUMO K; YUKI M
Number of Countries: 007 Number of Patents: 007
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 456199	A	19911113	EP 91107426	A	19910507	199146	B
JP 4226039	A	19920814	JP 91115464	A	19910419	199239	
JP 4226040	A	19920814	JP 91122272	A	19910424	199239	
EP 456199	A3	19920429	EP 91107426	A	19910507	199329	
US 5306651	A	19940426	US 91698092	A	19910510	199416	
EP 456199	B1	19970827	EP 91107426	A	19910507	199739	
DE 69127395	E	19971002	DE 627395	A	19910507	199745	
			EP 91107426	A	19910507		

Priority Applications (No Type Date): JP 90122938 A 19900515; JP 90120111 A 19900511
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 456199	A				
Designated States (Regional): DE FR GB IT NL					
JP 4226039	A		6	H01L-021/336	
JP 4226040	A		7	H01L-021/336	
US 5306651	A		14	H01L-021/265	
EP 456199	B1	E	13	H01L-021/84	
Designated States (Regional): DE FR GB IT NL					
DE 69127395	E			H01L-021/84	Based on patent EP 456199

Abstract (Basic): EP 456199 A

Prepn. process of polycrystalline semiconductor thin film transistors comprising: (i) non-single crystalline semiconductor formed on transparent insulating substrate, (ii) forming gate insulation layer and gate electrode on semiconductor, (iii) implanting impurity ions into source drain region of semiconductor using gate electrode as mask, (iv) irradiating with laser beams from rear surface of transparent insulating substrate thereby polycrystallising non-single crystalline semiconductor under gate electrode and channel regions simultaneously activating semiconductor at source drain region and without causing the semiconductor to be completely molten.

Preferred laser beam scanning speed is a beam spot dia x 5,000/sec or higher. Forming an active matrix substrate for producing a **liquid crystal display** device.

USE/ADVANTAGE - For use in production of polycrystalline thin film transistors used to drive image displaying devices, advantageous in that displays having large surface area can be produced having

plurality of thin film **products** on a single **substrate** which reduces **manufacturing** cost. (13pp Dwg.No.1/4)

Abstract (Equivalent): EP 456199 B

A process of preparing a polycrystalline semiconductor **thin film transistor**, comprising the steps of: forming a non-single crystalline semiconductor layer formed of amorphous silicon and having a thickness of 10-500 nm on a front surface side of a transparent insulating substrate; forming a gate insulation layer on the non-single crystalline semiconductor layer; forming a gate electrode of non-single crystalline semiconductor on the gate insulation layer at a channel region; implanting impurity ions into the gate electrode and a source-drain region of the non-single-crystalline semiconductor layer formed of amorphous silicon, where the gate electrode of semiconductor is used as a mask; irradiating continuous wave laser beams on the deposited semiconductor layers with a high scanning speed of a beam spot diameter x 5000/secondary or higher, and with a laser power between a first laser power threshold value for which the recrystallisation process begins and a second laser power threshold value for which the molten state begins, so that simultaneously the non-single crystalline semiconductor at the channel region is poly-crystallised, the non-single crystalline semiconductor at the source and drain region is poly-crystallised, the impurity ions implanted into the non-single crystalline semiconductor at the source-drain region are activated, and the impurity ions implanted into the gate electrode are activated and the non-single crystalline semiconductor of the gate electrode is poly-crystallised, without causing the non-single crystalline semiconductor layers to reach a completely molten state.

Dwg.4/4

Abstract (Equivalent): US 5306651 A

Preparing a polycrystalline semiconductor this film transistor comprises the steps: a forming a non-single crystalline semiconductor layer formed of amorphous silicon and having a thickness of 10-500nm on a front surface sick of a transparent substrate; forming a gate insulation layer on the non-single-crystalline semiconductor layer; forming a gate electrode of non-single crystalline semiconductor on the gate insulation layer at a channel region; implanting impurity ions into the gate electrode and a source-drain region of the non-single crystalline semiconductor layer formed of amorphous Si, in which the gate electrode of semiconductor is used as a mask, irradiating laser beams so that simultaneously the non-single crystalline semiconductor at the channel region is polycrystallised, the non-single crystalline semiconductor at the source and drain region is polycrystallised, the impurity ions implanted into the non-single crystalline semiconductor at the source-drain region are activated; and the impurity ions implanted into the gate electrode are activated and the non-single crystalline semiconductor of the gate electrodes is polycrystallised, without causing the non-single crystalline semiconductor layer to reach a molten state.

USE/ADVANTAGE - The transistor can be used for driving an image displaying device. The process increases productivity.

42/3,AB/3 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

07039944
THIN-FILM SEMICONDUCTOR DEVICE, AND METHOD FOR MANUFACTURING THE SAME

PUB. NO.: 2001-267578 [JP 2001267578 A]
PUBLISHED: September 28, 2001 (20010928)
INVENTOR(s): HAYASHI HISAO
APPLICANT(s): SONY CORP
APPL. NO.: 2000-075755 [JP 200075755]
FILED: March 17, 2000 (20000317)

ABSTRACT

PROBLEM TO BE SOLVED: To provide **substrates** suitable for the **manufacture** and product of a thin-film semiconductor device.

SOLUTION: A **substrate** 20 for **manufacture** with characteristics, capable of resisting of a process for forming a thin-film resistor 3 and a **substrate** 1 for the **product** with characteristics suitable for directly loading the **thin-film transistor** 3 are prepared in a preparation process. Next, the **substrate** 20 for **manufacture** is adhered to the **substrate** 1 for the **product**, so that the **substrate** 1 for the **product** can be supported from the back side in an adhering process. Then, at least the **thin-film transistor** 3 is formed on the surface of the **substrate** 1 for the **product** in a state that this is reinforced by the **substrate** 20 for **manufactured**. At least, the **substrate** 20 for **manufacturing** which is already used is isolated from the **substrate** 1 for the **product** in a isolating process.

47/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014591634
WPI Acc No: 2002-412338/200244
XRAM Acc No: C02-116449
TFT substrate and **manufacturing** method
Patent Assignee: SAMSUNG ELECTRONICS CO LTD (SMSU)
Inventor: JI H; SEO Y G
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
KR 2001111252	A	20011217	KR 200031830	A	20000609	200244	B

Priority Applications (No Type Date): KR 200031830 A 20000609
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
KR 2001111252	A		1	G02F-001/136	

Abstract (Basic): KR 2001111252 A
Abstract (Basic):
NOVELTY - A manufacturing method of a **TFT**(**Thin Film Transistor**) substrate is provided to decrease the number of masks on **manufacturing** a **TFT substrate** for an **LCD**(**Liquid Crystal Display**) and to improve an aperture ratio.
DETAILED DESCRIPTION - A gate line(22), a gate pad(24), a gate electrode and an ITO(Indium Tin Oxide) electrode(28) are formed through deposition of a conductive layer and dry or wet etching using a first mask. A photoresist is coated thereon with thickness of 1-2 micrometers. Photoresist patterns are formed by beam emitting and developing of the photoresist through a second mask. The intermediate layer and the semiconductor layer of a data line part are removed to expos the gate insulating film. A conductive layer pattern for source/drain of a channel part and an intermediate layer pattern are etched, and the photoresist pattern is etched to form data lines(62,64,65,66,68). After that, a passivation is formed through CVD of SiNx or spin coating of **organic** insulating material. The passivation is etched together with the gate insulating film by using a third mask to form contact holes(71,72,73,74) for exposing the drain electrode(66), the gate pad(24), the data pad(64) and a conductive layer pattern(68). Finally, a pixel electrode(82), an auxiliary gate pad(84) and an auxiliary data pad(86) are formed through deposition of an ITO layer and photolithography using a fourth mask.
pp; 1 DwgNo 1/10

47/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014499462
WPI Acc No: 2002-320165/200236
XRAM Acc No: C02-093006
XRPX Acc No: N02-250713
Liquid crystal display device and its manufacture
Patent Assignee: NEC CORP (NIDE)
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2001324708	A	20011122	JP 2000377162	A	20001212	200236	B
KR 2001088329	A	20010926	KR 20016613	A	20010210	200236	

Priority Applications (No Type Date): JP 200062284 A 20000307
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2001324708	A		11	G02F-001/1333	
KR 2001088329	A			G02F-001/136	

Abstract (Basic): JP 2001324708 A
Abstract (Basic):
NOVELTY - A **liquid crystal display** device has a **thin film transistor** substrate having the **thin film transistor** of an active element, a substrate facing the **thin film transistor** substrate and having an electrode sharing each pixel, and a liquid crystal layer filled between the substrates.
DETAILED DESCRIPTION - The **thin film transistor** substrate has a first transparent substrate, and a first glare protection film, an underlying film, a **thin film transistor**, a first interlayer insulating film, a wiring metal film, a second interlayer insulating film, a third interlayer insulating film, a flattening film, a first transparent electrode film, and a first alignment layer formed in that order on the first transparent substrate. The substrate facing the **thin film transistor** substrate has a second transparent substrate, and a second transparent electrode, and a second alignment layer formed in that order on the second transparent substrate. The flattening film consists of a transparent resin absorbing no light having a wavelength of 300 nm or more.
USE - The method manufactures the **liquid crystal display** device.
ADVANTAGE - The method disposes the glare protection film on at least one side of the **thin film transistor** on the **thin film transistor** substrate and forms by thermal polymerization the flattening film formed by using the transparent acrylic resin and having no light absorption at a wavelength of 30 nm or more under the transparent electrode of the **thin film transistor** substrate. The resulting advantages include: (a) deteriorating or coloring no flattening film even if ultraviolet rays

having a wavelength of 300 nm or more is leaked from the filter of a light source, including a high powder projector; forming the flattening film by the thermal polymerization exists no photosensitive group absorbing light having a wave length of 300 nm or more, eliminating the need for irradiation treatment to ultravilolet light having high energy to damage no flattening film or to develop no bubbles; (b) deteriorating no image quality since no light is incident on the **thin film transistor**; by the use of the flattening film, relaxing irregularities which would otherwise be generated by laminating the glare protection films, developing no unusual alignment of a liquid crystal molecule to prevent development of reverse twist, reverse tilt.

47/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014498051
WPI Acc No: 2002-318754/200236
XRPX Acc No: N02-249329
Heat processing monitor unit used in manufacture of e.g. **liquid crystal display**, has structure in which semiconductor and metal contact are set through opening of insulating film
Patent Assignee: MATSUSHITA DENKI SANGYO KK (MATU)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2001274213	A	20011005	JP 200086120	A	20000327	200236	B

Priority Applications (No Type Date): JP 200086120 A 20000327
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2001274213	A		9	H01L-021/66	

Abstract (Basic): JP 2001274213 A
Abstract (Basic):
NOVELTY - The heat processing monitor unit has a structure in which a semiconductor and a metal contact are set through the opening of an insulating film.
USE - Used semiconductor **substrate** processing during **manufacture** of e.g. **LCD**, EL display.
ADVANTAGE - Evaluates actual heat processing and in-plane uniformity of substrate. Can be used for performance evaluation and stability of thermal treatment equipment. Improves image quality of **organic** EL display and ensures high homogeneity of **LCD** due to highly efficient **TFT** substrate processing.
DESCRIPTION OF DRAWING(S) - The figure shows the heat processing monitor unit. Drawing includes non-English language text.
pp; 9 DwgNo 1/9

47/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014433904
WPI Acc No: 2002-254607/200230
XRPX Acc No: N02-196684
Thin film transistor array **substrate** **manufacturing** method for display devices, involves correcting size of primary pattern based on deformation amount of substrate
Patent Assignee: TOSHIBA KK (TOKE); NINOMIYA T (NINO-I)
Inventor: NINOMIYA T
Number of Countries: 003 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20010029055	A1	20011011	US 2001814962	A	20010323	200230	B
KR 2001093064	A	20011027	KR 200114615	A	20010321	200230	
JP 2001272929	A	20011005	JP 200085103	A	20000324	200230	

Priority Applications (No Type Date): JP 200085103 A 20000324
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20010029055	A1		15	H01L-021/00	
KR 2001093064	A			G02F-001/136	
JP 2001272929	A		7	G09F-009/30	

Abstract (Basic): US 20010029055 A1
Abstract (Basic):
NOVELTY - A primary pattern is formed on a glass substrate (1) by correcting in advance the size of the pattern based on an amount of deformation of the substrate. Another pattern is formed on the substrate in conformity with the primary pattern by collecting exposing a film (3) formed on the substrate to light by using a gate electrode (4) used as mask.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for display device manufacturing method.

USE - For manufacturing polycrystalline silicon **thin film transistor** array substrate for display devices such as active matrix type **liquid crystal display** (**LCD**) devices and **organic** electroluminescence (EL) display devices in notebook computer.

ADVANTAGE - A pattern of a predetermined shape is formed finally even if the substrate is deformed during the manufacturing steps, by correcting the size of the pattern and hence the occurrence of defective display is prevented. Enables **manufacturing** an array **substrate** of a high reliability and high yield.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of **liquid crystal display** device manufactured by using a **TFT** array substrate.

Glass substrate (1)
Film (3)
Gate electrode (4)
pp; 15 DwgNo 3/13

47/3,AB/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014353440
WPI Acc No: 2002-174141/200223
XRAM Acc No: C02-053991
XRPX Acc No: N02-132036
Developing solution, used for image formation, for manufacturing of color filter, for a color filter-bearing active matrix substrate and for a **liquid crystal display** device, and comprises a specific compound
Patent Assignee: FUJI PHOTO FILM CO LTD (FUJF)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2001215730	A	20010810	JP 200022280	A	20000131	200223	B

Priority Applications (No Type Date): JP 200022280 A 20000131
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2001215730	A		23	G03F-007/32	

Abstract (Basic): JP 2001215730 A
Abstract (Basic):
NOVELTY - Developing solution contains a specific compound.
DETAILED DESCRIPTION - Developing solution contains a compound of formula (I).
INDEPENDENT CLAIMS are also included for: (1) a method of image formation; (2) the manufacture of a color filter; (3) the manufacture of an color filter-bearing active matrix substrate; and (4) a **liquid crystal display** device.
R=H, (un)substituted 1-6C alkyl;
A, B=1-6C divalent hydrocarbon;
X=divalent linkage group; and
p=0 or 1.
USE - The developing solution are used for the image formation and for manufacturing the color filter and the color filter-bearing active matrix substrate and the **liquid crystal display** device.
ADVANTAGE - The developing solution causes no adverse effects on a **thin film transistor**, and forms the image having high definition, and has superior aging stability. No decrease in development caused by a variation in pH is observed in development.
pp; 23 DwgNo 0/0

47/3,AB/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014195426
WPI Acc No: 2002-016123/200202
XRAM Acc No: C02-004125
Method for **manufacturing substrate** of **thin film transistor** for **liquid crystal display**
Patent Assignee: SAMSUNG ELECTRONICS CO LTD (SMSU)
Inventor: PARK Y B
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
KR 2001057663	A	20010705	KR 9961034	A	19991223	200202	B

Priority Applications (No Type Date): KR 9961034 A 19991223
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
KR 2001057663	A		1	H01L-029/786	

Abstract (Basic): KR 2001057663 A
Abstract (Basic):
NOVELTY - A method for **manufacturing** a **substrate** of a **thin film transistor**(**TFT**) for a **liquid crystal display**(**LCD**) is provided to improve step coverage and prevent the number of processing steps, by using copper as an interconnection to prevent signal delay, and by forming the interconnection as a dual layer to prevent a short circuit while using a metal **organic** chemical vapor deposition(MOCVD) method.
DETAILED DESCRIPTION - A gate interconnection(21,22,23) is formed on an insulating substrate(10). The first insulation layer is formed to cover the gate interconnection. A semiconductor layer(40) is formed on the first insulation layer. A data interconnection(61,62,63,64) including a data line, a source electrode and a drain electrode is formed on the first insulation layer. The second insulation layer has a contact hole covering the data interconnection and exposing the drain electrode. A pixel electrode is connected to the drain electrode through the contact hole. At least one of the processes for forming the gate interconnection and the data interconnection includes a process for forming the first conduction layer and a process for forming the second conduction layer on the first conduction layer by a metal **organic** chemical vapor deposition(MOCVD) method.
pp; 1 DwgNo 1/10

47/3,AB/7 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013087793
WPI Acc No: 2000-259665/200023
XRAM Acc No: C00-079646
XRPX Acc No: N00-193208
Active matrix **substrate manufacturing** method for **liquid crystal display** devices, involves performing plasma treatment on surface of **organic** insulating film using nitrogen gas
Patent Assignee: SHARP KK (SHAF)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 11337973	A	19991210	JP 98148014	A	19980528	200023	B

Priority Applications (No Type Date): JP 98148014 A 19980528
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 11337973	A		9	G02F-001/136	

Abstract (Basic): JP 11337973 A
NOVELTY - An **organic** insulating film (9) covers a **TFT** and wiring formed on insulation substrate (6). Plasma treatment is performed on the surface of the film using nitrogen gas. A pixel electrode (10) is formed which electrically connects the **TFT** via a contact hole (8) on the insulating film.
USE - For **liquid crystal display** devices used in notebook type personal computer.
ADVANTAGE - Pixel electrode is sufficiently adhered on the **organic** insulating film. As the film thickness of pixel electrode is optimized, transmittance of **LCD** device is improved. Leak between pixel electrodes is predetermined and reduction in power consumption is achieved. DESCRIPTION OF DRAWING(S) - The figure shows the sectional view of stages in **manufacturing** an active matrix **substrate**. (6) Insulation substrate; (8) Contact hole; (9) **Organic** insulating film; (10) Pixel electrode.
Dwg.4/7

47/3,AB/8 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012937281
WPI Acc No: 2000-109128/200010
XRAM Acc No: C00-033070
XRPX Acc No: N00-083871
Active matrix substrate used in **liquid crystal display** device - has **organic** interlayer films formed between pixel electrode and wiring, which covers source electrode, source wiring, drain electrode and back channel
Patent Assignee: NEC CORP (NIDE); NIPPON ELECTRIC CO (NIDE)
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 11307778	A	19991105	JP 98113659	A	19980423	200010	B
KR 99083412	A	19991125	KR 9914449	A	19990422	200055	

Priority Applications (No Type Date): JP 98113659 A 19980423
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 11307778	A		8	H01L-029/786	
KR 99083412	A			G02F-001/1333	

Abstract (Basic): JP 11307778 A

NOVELTY - **Organic** interlayer films (8a,8b) which covers source electrode (6a), source wiring (6b), a drain electrode (7) and a back channel directly, are formed between pixel electrode (9) and wiring. The direct **organic** layer insulating film of sublayer contacts channel of **TFT** (10). DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for active matrix **substrate manufacturing** method.

USE - In active matrix **LCD** device.

ADVANTAGE - Since **organic** interlayer film with low relative dielectric constant is formed, crosstalk occurring during wiring by pixel electrode and floating capacitance is suppressed, thereby production cost of **LCD** device is greatly reduced. DESCRIPTION OF DRAWING(S) - The figure shows the top and sectional views of active matrix substrate in **LCD** device. (6a) Covers source electrode; (6b) Source wiring; (7) Drain electrode; (8a,8b) **Organic** interlayer films; (9) Pixel electrode; (10) **TFT**.

Dwg.1/6

47/3,AB/9 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011473600
WPI Acc No: 1997-451507/199742
Related WPI Acc No: 1998-123279
XRAM Acc No: C97-144058
XRPX Acc No: N97-376188
Transistor substrate for **liquid crystal display** - comprises transistor, over substrate, having gate, source, drain, semiconductor layer and gate insulation layer, and protection film, over transistor, including specific material
Patent Assignee: LG ELECTRONICS INC (GLDS); KINSEISHA KK (GLDS); LG PHILIPS LCD CO LTD (GLDS)
Inventor: KIM J; KIM W; LEE H; LIM K; LYU K; PARK S; KIM J H; KIM W K; LEE H Y; LIM K N; LYU K H; PARK S I; RYU K; LIM G N; KIM W G; RYOO G H; HA Y; OH Y
Number of Countries: 006 Number of Patents: 017
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
GB 2311653	A	19971001	GB 976354	A	19970326	199742	B
FR 2746961	A1	19971003	FR 973615	A	19970325	199747	
DE 19712233	A1	19971030	DE 1012233	A	19970324	199749	
JP 10041519	A	19980213	JP 9791520	A	19970326	199817	
KR 97066694	A	19971013	KR 979366	A	19970319	199842	
KR 98003740	A	19980330	KR 9622404	A	19960619	199903	
KR 98003743	A	19980330	KR 9623295	A	19960624	199903	
KR 98003744	A	19980330	KR 9623296	A	19960624	199903	
KR 98003745	A	19980330	KR 9623448	A	19960625	199903	
GB 2311653	B	19990804	GB 976354	A	19970326	199933	
US 6100954	A	20000808	US 97826804	A	19970325	200040	
KR 229609	B1	19991115	KR 9623296	A	19960624	200111	
KR 229612	B1	19991115	KR 9623295	A	19960624	200111	
KR 232681	B1	19991201	KR 9622404	A	19960619	200111	
KR 232682	B1	19991201	KR 9623448	A	19960625	200111	
US 6211928	B1	20010403	US 97826084	A	19970325	200120	
			US 97872368	A	19970610		
KR 255590	B1	20000501	KR 979366	A	19970319	200128	

Priority Applications (No Type Date): KR 9623448 A 19960625; KR 968344 A 19960326; KR 9622404 A 19960619; KR 9623295 A 19960624; KR 9623296 A 19960624; KR 9636947 A 19960830
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
GB 2311653	A		83	G02F-001/136	
FR 2746961	A1		65	H01L-021/312	
DE 19712233	A1		52	H01L-029/786	
JP 10041519	A		27	H01L-029/786	
KR 97066694	A			G02F-001/136	
KR 98003740	A			G02F-001/136	
KR 98003743	A			G02F-001/136	
KR 98003744	A			G02F-001/136	

KR 98003745	A	G02F-001/136	
GB 2311653	B	G02F-001/136	
US 6100954	A	G02F-001/1333	
KR 229609	B1	G02F-001/136	
KR 229612	B1	G02F-001/136	
KR 232681	B1	G02F-001/136	
KR 232682	B1	G02F-001/136	
US 6211928	B1	G02F-001/136	CIP of application US 97826084 CIP of patent US 6100954
KR 255590	B1	G02F-001/136	

Abstract (Basic): GB 2311653 A

A transistor substrate for a **liquid crystal display** (**LCD**) comprises: (a) a substrate (111); (b) a transistor, over the substrate, having a gate (113), a source (121, 123), a drain (121, 127), a semiconductor layer (119) and a gate insulation layer (157); and (c) a protection film (159), over the transistor, including a material derived from fluorinated polyimide, Teflon (RTM), Cytop (RTM), fluoro polyaryl ether, fluorinated para-xylene, perfluoro cyclobutane (PFCB) or benzocyclobutene (BCB).

Also claimed are: (i) a transistor substrate as above in which the gate insulation layer (157) includes a material derived from fluorinated polyimide, Teflon (RTM), Cytop (RTM), fluoro polyaryl ether, fluorinated para-xylene, PFCB or BCB; (ii) a method for **manufacturing** the transistor **substrate** which comprises forming the transistor over the substrate (111) and forming the protection film (159) over the transistor; (iii) a semiconductor device insulating layer as above; (iv) a semiconductor switching device for a **LCD** where the gate insulation layer and/or the protection layer comprise an insulating layer as above; (v) a **thin film transistor** for a **LCD**, where the gate insulation layer and/or the protection layer comprise an insulating layer as above; and (vi) a method of manufacturing a semiconductor device which comprises spin coating an insulating layer as above.

ADVANTAGE - The **LCD** does not have a stepped profile due to a multilayered structure. It has less parasitic capacitance and is free from electron trap and poor adhesion at the interface between the insulation and semiconductor layers. The gate insulation layer has a smooth surface which prevents problems such as line disconnection and/or short circuit. Even though the gate insulation layer is thin, it has sufficient insulation property. The application of an **organic** film on the gate electrode does not affect the function of a **thin film transistor**. This is because the thickness of the **organic** film is reduced to compensate the low dielectric constant of the **organic** film. Due to the low dielectric constant of the **organic** material, spaces or gaps between pixel electrodes and gate and signal bus lines are not required. Consequently, it is possible to form a wider pixel electrode than in conventional methods. This yields an improved aperture ratio and high quality contrast can be achieved.

47/3,AB/10 (Item 10 from file: 347)
DIALOG(R)File 347:JAPIO

06018407
LIQUID CRYSTAL DISPLAY SUBSTRATE AND ITS **MANUFACTURE**

PUB. NO.: 10-301507 [JP 10301507 A]
PUBLISHED: November 13, 1998 (19981113)
INVENTOR(s): MAEDA HIROSHI
APPLICANT(s): MATSUSHITA ELECTRIC IND CO LTD [000582] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 09-107977 [JP 97107977]
FILED: April 25, 1997 (19970425)

ABSTRACT

PROBLEM TO BE SOLVED: To greatly decrease the product cost and to obtain superior stable display quality by providing an insulating substrate constituted so that the electric connection point between a transparent pixel electrode and the electrode part of a switching element is positioned on an electrode wire.

SOLUTION: On the insulating substrate 11 as a transparent substrate, scanning signal wires 12, a gate insulating film 13 on the scanning signal wires 12, and an image signal wire 14, a **TFT** 15 as a switching element, and a drain electrode 19 in the layer above the gate insulating film 13 are provided. A colored layer 17 is positioned on the drain electrode 19 and a light shield film 18 is at the periphery of the colored layer 17; and a pixel electrode 16 is provided on the colored layer 17. Consequently, an array substrate AR1 and a counter substrate are reduced in position shift when stuck together, and the **liquid crystal display** panel having a higher aperture rate is actualized. Further, the **manufacture** of a **substrate** for the colored layer 17 and its high-precision sticking process can be eliminated

47/3,AB/11 (Item 11 from file: 347)
DIALOG(R)File 347:JAPIO

05631759
THIN FILM TRANSISTOR ARRAY **SUBSTRATE** AND ITS **MANUFACTURE**

PUB. NO.: 09-246559 [JP 9246559 A]
PUBLISHED: September 19, 1997 (19970919)
INVENTOR(s): YAMAGUCHI AYAKO
HIROSE TAKASHI
ONISHI HIROYUKI
APPLICANT(s): MATSUSHITA ELECTRIC IND CO LTD [000582] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 08-053583 [JP 9653583]
FILED: March 12, 1996 (19960312)

ABSTRACT

PROBLEM TO BE SOLVED: To materialize an excellent grade of indication by improving the numerical aperture of a **liquid crystal display**, and also, controlling the nonorientation area.

SOLUTION: Negative coloring photosensitive resin 2 where pigment and carbon particles are dispersed is applied on a glass board 1 where thin film transistors and picture element electrodes are arranged in matrix form, and it is exposed to an ultraviolet ray 4 through a photomask 3. This is soaked in developer 5, and developer is replaced with rinsing solution before the termination of development, and replacement cleaning is performed with high-pressure jet so as to get negative coloring photosensitive resin 9. Hereby, the edge part 28 of the negative coloring photosensitive resin pattern 11 to serve as a light shield layer can be patterned in the shape of an outward taper, and a nonorientation area can be controlled enough

47/3,AB/12 (Item 12 from file: 347)
DIALOG(R)File 347:JAPIO

05515082

THIN FILM TRANSISTOR ARRAY **SUBSTRATE**, ITS **MANUFACTURE**, AND **LIQUID CRYSTAL DISPLAY**

PUB. NO.: 09-129882 [JP 9129882 A]
PUBLISHED: May 16, 1997 (19970516)
INVENTOR(s): YAMAGUCHI AYAKO
TSUTSU HIROSHI
APPLICANT(s): MATSUSHITA ELECTRIC IND CO LTD [000582] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 07-281799 [JP 95281799]
FILED: October 30, 1995 (19951030)

ABSTRACT

PROBLEM TO BE SOLVED: To realize excellent display quality, by improving the aperture ratio of a liquid display, and sufficiently restraining reflection of external light on the display image surface.

SOLUTION: Negative photoresist 2 in which black **organic** pigment is dispersed is spread on a substrate 1 on which thin film transistors and picture element electrodes are arranged in a matrix, and exposed to UV rays 4 via a photomask 3. A colored photoresist pattern 7 is obtained by developing. Fine unevenness is formed on the surface of the colored photoresist pattern 7 by oxygen plasma treatment, and a colored photoresist pattern 8 is obtained. By using a **thin film transistor** array substrate and forming a liquid display, alignment precision is improved as compared with one provided with a light shielding layer on the facing substrate side, and the aperture ratio can be improved. Since fine unevenness is formed on the colored photoresist pattern 8 turning to a light shielding layer, reflection of external light on the display image surface can be sufficiently restrained.

47/3,AB/13 (Item 13 from file: 347)
DIALOG(R)File 347:JAPIO

04737137
MANUFACTURE OF **THIN FILM TRANSISTOR** MATRIX

PUB. NO.: 06-208137 [JP 6208137 A]
PUBLISHED: July 26, 1994 (19940726)
INVENTOR(s): OZAKI KIYOSHI
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 05-003640 [JP 933640]
FILED: January 13, 1993 (19930113)

ABSTRACT

PURPOSE: To improve the reliability of element, and to improve the yield of the manufacture by forming contact holes, which are to be opened in a second insulating layer, into the normal taper shape, and preventing the conductivity of the surface of a **substrate** in the **manufacture** of a **thin film transistor**(**TFT**) matrix.

CONSTITUTION: A gate electrode 2 and a stored capacity lower electrode 3 are formed on a substrate 1 made of the transparent and insulating material, and a first insulating thin film 4 and an operating semiconductor layer 5 and a channel protecting film 6 are formed thereon in order. A contact layer 7 and a metal film 8 are formed in order on the substrate a parts except for the channel protecting film 6 immediately on the gate electrode 2, and patterning is performed to form a drain electrode 8D and a source electrode 8S and a stored capacity upper electrode 8C. The substrate is covered with a second insulating film 9 made of the transparent resin, and the second insulating film 9 is formed with contact holes, and a transparent electrode film is formed on the substrate and made to contact with the stored capacity upper electrode 8C and the source electrode 8B, and patterning is performed to form a picture element electrode 11

47/3,AB/14 (Item 14 from file: 347)
DIALOG(R)File 347:JAPIO

04670909
METHOD OF **MANUFACTURING LIQUID CRYSTAL DISPLAY SUBSTRATE**

PUB. NO.: 06-342809 [JP 6342809 A]
PUBLISHED: December 13, 1994 (19941213)
INVENTOR(s): KASAI TSUTOMU
KOSHIMO TOSHIYUKI
KIKUCHI MASAHITO
NAKATANI MITSUO
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 05-131605 [JP 93131605]
FILED: June 02, 1993 (19930602)

ABSTRACT

PURPOSE: To prevent wire disconnection, shortcircuit or point defect caused by flakes or foreign substances in a finished **TFT** by washing a semiconductor layer with a washing liquid containing an **organic** alkali after a semiconductor layer has been formed.

CONSTITUTION: After an oxide silicon film SIO is provided on both sides of a lower transparent glass substrate SUB1, a first conductivity film g1 made of chrome is provided on it. The first conductivity film g1 is selectively etched to form a gate terminal GTM and a drain terminal. Then, a second conductivity film g2 made of Aluminum-Palladium is provided. The second conductivity film g2 is anode-oxidized to provide an anode oxide film AOF on a scanning signal line GL. Hydrogen gas is introduced into a plasma CVD unit to provide an N(+)-type amorphous silicon film. Then, the N(+)-type amorphous layer is washed with **organic** alkali liquid. Thus, it is possible to remove flakes or foreign substances adhering to the surface of the semiconductor layer.

47/3,AB/15 (Item 15 from file: 347)
DIALOG(R)File 347:JAPIO

04494585
LIQUID CRYSTAL DISPLAY DEVICE AND ITS MANUFACTURE

PUB. NO.: 06-138485 [JP 6138485 A]
PUBLISHED: May 20, 1994 (19940520)
INVENTOR(s): TAKAHASHI EIICHI
APPLICANT(s): SHARP CORP [000504] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 04-289101 [JP 92289101]
FILED: October 27, 1992 (19921027)
JOURNAL: Section: P, Section No. 1787, Vol. 18, No. 439, Pg. 77, August 16, 1994 (19940816)

ABSTRACT

PURPOSE: To provide the **liquid crystal display** device and its manufacture which can eliminate a display defect due to a light leak and a display defect resulting from the fitting of a polarizing plate.

CONSTITUTION: At the point of time when a base substrate 1 and an opposite **substrate** 2 are **manufactured** , the performance of the base substrate 1 is inspected. If a defect of a **TFT** is confirmed by this inspection, a colored **organic** light shield film 16 is formed on a defective pixel electrode 9 connected to the defective **TFT** and/or a counter electrode 12 on the opposite substrate 2 corresponding to the defective pixel electrode 9. Consequently, light to pass through the defective pixel electrode 9 can completely be cut off.

47/3,AB/16 (Item 16 from file: 347)
DIALOG(R)File 347:JAPIO

03944827
MANUFACTURE OF ACTIVE MATRIX **SUBSTRATE** AND **LIQUID CRYSTAL DISPLAY** ELEMENT USING THE SAME

PUB. NO.: 04-309927 [JP 4309927 A]
PUBLISHED: November 02, 1992 (19921102)
INVENTOR(s): KOSHIMO TOSHIYUKI
YORITOMI YOSHIFUMI
TAKANO TAKAO
NAKATANI MITSUO
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 03-076083 [JP 9176083]
FILED: April 09, 1991 (19910409)
JOURNAL: Section: P, Section No. 1503, Vol. 17, No. 129, Pg. 134, March 18, 1993 (19930318)

ABSTRACT

PURPOSE: To reduce the manufacturing cost by decreasing all forming processes of switching elements, electric conductors, and picture element electrodes which constitute the active matrix substrate.

CONSTITUTION: A gate electrode 2 is formed by plating on a transparent substrate 1 whose surface is made of an insulator, an **organic** insulator such as polyimide is applied and set to form a gate insulating film 3, and an **organic** semiconductor is printed thereupon to form a semiconductor layer 4. A channel protection film 23 is formed at the part of a **thin film transistor** which becomes a channel and a source electrode 5 and a drain electrode 6 are formed by plating. Lastly, a picture element electrode 7 is formed by printing.

47/3,AB/17 (Item 17 from file: 347)
DIALOG(R)File 347:JAPIO

02761614
MANUFACTURE OF **THIN FILM TRANSISTOR** ACTIVE MATRIX SUBSTRATE

PUB. NO.: 01-059214 [JP 1059214 A]
PUBLISHED: March 06, 1989 (19890306)
INVENTOR(s): KANEKO HIROSHI
KONISHI NOBUTAKE
SUZUKI TAKAYA
MIMURA AKIO
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 62-215403 [JP 87215403]
FILED: August 31, 1987 (19870831)
JOURNAL: Section: P, Section No. 887, Vol. 13, No. 266, Pg. 43, June 20, 1989 (19890620)

ABSTRACT

PURPOSE: To **manufacture** an active matrix **substrate** with a flat surface where there is no trouble even when thin film transistors, scanning wiring, and signal wiring are mounted by polishing away an unnecessary insulator sticking on the surface of the substrate when an insulating filler is charged in a pinhole part on the surface of the substrate.

CONSTITUTION: A pinhole flawed part 16 is filled with the liquid filler and heat-treated in an acid or inert atmosphere to obtain an insulator 17. The filler is prepared by dissolving **organic** metal, etc., into a solvent, a glass substrate 18 is dipped, and deaeration is carried out with an ultrasonic wave or by vacuum suction, etc., to fill the pinhole flawed part 16. The insulator 17 formed swelling on the surface of the substrate 18 is polished away finally to charge the insulator 17 only in the flawed part selectively. Consequently, the transparent insulating substrate having no pinhole in the surface is obtained and the thin film active matrix **substrate** is **manufactured** which has no characteristic deterioration even when electrode wiring for thin film transistors, scanning, signals, etc., is provided.

47/3,AB/18 (Item 18 from file: 347)
DIALOG(R)File 347:JAPIO

01588365
MANUFACTURE OF **THIN FILM TRANSISTOR**

PUB. NO.: 60-066865 [JP 60066865 A]
PUBLISHED: April 17, 1985 (19850417)
INVENTOR(s): MURAKI AKIRA
APPLICANT(s): TOPPAN PRINTING CO LTD [000319] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 58-176716 [JP 83176716]
FILED: September 24, 1983 (19830924)
JOURNAL: Section: E, Section No. 337, Vol. 09, No. 204, Pg. 24, August 21, 1985 (19850821)

ABSTRACT

PURPOSE: To prevent the damage of the surface of a substrate and to block the diffusion of alkaline components from the substrate by a method wherein an **organic** polymer layer by plasma polymerization is formed on the substrate, when the **thin film transistor** is formed on the transparent substrate of glass or quartz.

CONSTITUTION: An **organic** polymer film 8 of hydrocarbon series is formed on the transparent substrate 1 made of glass or quartz by the reduced pressure glow discharge of a hydrocarbon gas of methane, ethane, acetylene, ethylene or benzene. Next, a gate electrode 2 is provided at the center of this surface and then covered with a gate insulation layer 6, and an amorphous Si layer 5 is provided thereon into said transistor. Such a manner allows no decrease in the transparency due to the damage of the **substrate** 1 during the **manufacturing** process of the transistor because the chemical properties of the film 8 are extremely stable, and facilitates the manufacture because of durability to a temperature of approximately 400c.

60/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014261568
WPI Acc No: 2002-082266/200211
XRAM Acc No: C02-024785
XRPX Acc No: N02-061302
Manufacture of array panel for use in **liquid crystal display** device, involves etching semiconductor layer and leaving gate insulating layer on gate line
Patent Assignee: LG PHILIPS LCD CO LTD (GLDS); KIM H (KIMH-I); MOON K (MOON-I)
Inventor: KIM H S; MUN G H; KIM H; MOON K
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20010034073	A1	20011025	US 2000734562	A	20001213	200211 B
KR 2001055982	A	20010704	KR 9957330	A	19991213	200211

Priority Applications (No Type Date): KR 9957330 A 19991213
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20010034073	A1		11	H01L-021/00	
KR 2001055982	A			G02F-001/136	

Abstract (Basic): US 20010034073 A1
Abstract (Basic):
NOVELTY - Manufacture of an array panel comprises etching a first interstructure using a photoresist pattern to leave the photoresist and the layers under the photoresist over data line and to leave the etched semiconductor layer and gate insulating layer over the gate line to define a second interstructure; and etching the second interstructure to leave the gate insulating layer on gate line.
DETAILED DESCRIPTION - Manufacture of an array panel comprises forming a gate line (113) on a substrate using a first mask. A gate insulating layer (115), a doped semiconductor layer (117), and a metal layer are formed sequentially on the whole substrate while covering the gate line. A data line (119) and an island shaped metal portion (121) are formed on the semiconductor layer over the gate line by patterning the metal layer using a second mask. A protection layer is formed on the semiconductor layer while covering the data line and the island shaped metal portion. A photoresist pattern is formed on the protection layer over the data line using a third mask to define a first interstructure. Etching the first interstructure using the photoresist pattern to leave the photoresist and the layers under the photoresist over the data line and to leave the etched semiconductor layer and the gate insulating layer over the gate line to define a second interstructure. The second interstructure is etched to leave the gate insulating layer on the gate line. Finally, a **pixel electrode** is formed covering a portion of the gate insulating layer on the gate line using a fourth mask.
USE - For manufacturing an array panel for use in a **liquid**

crystal display device.

ADVANTAGE - Etching only the semiconductor layer on the gate insulating layer makes it easy to obtain a gate insulating layer having a uniform thickness. Since the gate insulating layer acts as a dielectric layer for capacitor, uniform thickness of the gate insulating layer on the gate line independent of the position of the pixel region leads to a constant capacitance of the capacitor throughout the whole pixel regions.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of an array **substrate** during its **manufacture**.

Gate line (113)
Gate insulating layer (115)
Semiconductor layer (117)
Data line (119)
Island shaped metal portion (121)
pp; 11 DwgNo 3B/4

60/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014208215
WPI Acc No: 2002-028912/200204
XRAM Acc No: C02-008166
XRPX Acc No: N02-022404

Manufacture of microlens **substrate** used in liquid crystal panels, involves hardening a resin placed in concave cavity of a substrate

Patent Assignee: SEIKO EPSON CORP (SHIH)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2001141907	A	20010525	JP 99323165	A	19991112	200204	B

Priority Applications (No Type Date): JP 99323165 A 19991112
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2001141907	A		15	G02B-003/00	

Abstract (Basic): JP 2001141907 A
Abstract (Basic):

NOVELTY - A resin layer (9) is provided on a substrate (2) with several concave portions (3). Another substrate (8) is then placed on the resin layer and the resin is hardened to form microlens (4) in the concave portions. The resin had a rate of shrinkage of 8.8% or less before hardening.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following: (i) Microlens substrate (1); (ii) Opposing substrate (10) for liquid crystal panels (16) which has a transparent electrically conductive film (12) provided on substrate (2) or (8); (iii) Liquid crystal panel; and (iv) Projection type display device which has a light valve through which an image is projected.

USE - For opposing substrates of liquid crystal panels and projection type display devices (all claimed).

ADVANTAGE - The microlens substrate has high ultraviolet rays resistance. Generation of defects, air bubbles, peeling and cloudiness are prevented.

DESCRIPTION OF DRAWING(S) - The figure shows the cross-sectional view of liquid crystal panel.

Microlens substrate (1)
Substrates (2,8)
Concave portion (3)
Microlens (4)
Resin layer (9)
Opposing substrate (10)
Black matrix (11)
Transparent film (12)
Liquid crystal panel (16)
TFT substrate (17)
Pixel electrode (172)

60/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013796410
WPI Acc No: 2001-280621/200129
XRAM Acc No: C01-085087
XRPX Acc No: N01-200035
Manufacturing **liquid crystal display**, by forming light developable organic layer over substrate surface, and removing residual portion of light developable organic layer remaining on drain electrode and data pad
Patent Assignee: LG LCD INC (GLDS)
Inventor: KIM J H; KIM W K; PARK J Y
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6204081	B1	20010320	US 99315650	A	19990520	200129	B

Priority Applications (No Type Date): US 99315650 A 19990520
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6204081	B1		12	H01L-021/00	

Abstract (Basic): US 6204081 B1
Abstract (Basic):
NOVELTY - A **liquid crystal display** (**LCD**) is manufactured by forming a light developable organic layer over substrate surface on which thin film transistor is formed, and removing a residual portion of the light developable organic layer remaining on surface of drain electrode and data pad and exposing surface of gate pad.
DETAILED DESCRIPTION - Manufacturing an **LCD** comprises forming a thin film transistor over a substrate, forming a light developable organic layer over an entire surface of the substrate, partially exposing a part of drain electrode, data pad, and gate insulating layer over a gate pad, and forming a transparent conductive layer in contact with the exposed drain electrode, data pad, and gate pad and which covers a part of the surface of the etched light developable organic layer. The thin film transistor comprises the drain electrode (170d), data pad (170c) and data insulating layer over the gate pad (160b).
USE - For manufacturing **LCD**.
ADVANTAGE - By using the light developable BCB protection layer, there is no need to apply a photoresist in order to pattern the light protection layer. The occurrence of the jagged protruding portion or other developable protection later caused by an error in the thickness of the applied photoresist is prevented thus the manufacturing of the **LCD** is simplified compared to conventional method. The **pixel electrodes** can be patterned accurately and defective patterning of the pinhole of the **pixel electrode** is prevented.
DESCRIPTION OF DRAWING(S) - The figure is a cross-sectional views illustrating **manufacturing** steps of a **substrate**.
Storage capacitance electrode (135)

60/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012443465
WPI Acc No: 1999-249573/199921
XRPX Acc No: N99-186185
TFT **substrate manufacturing** method for **LCD** device used in TV - involves forming source-drain **electrodes** on **pixel electrode** using photoresist as mask
Patent Assignee: MATSUSHITA DENKI SANGYO KK (MATU)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 11072802	A	19990316	JP 97235163	A	19970829	199921	B

Priority Applications (No Type Date): JP 97235163 A 19970829
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 11072802	A		6	G02F-001/136	

Abstract (Basic): JP 11072802 A

NOVELTY - The photosensitive resist is coated on the **pixel electrode** material (5) and exposure and development is carried out. The source-drain electrodes are formed on the **pixel electrode** material and connected to TFTs through the contact holes (4a). DETAILED DESCRIPTION - The drive TFTs are formed on a substrate (1). The insulation film (4) is coated on the substrate by exposing it to the adhesion reinforcement agent (10). The contact holes (4a) are formed in the insulation film by executing exposure and development on it using the photomask with specific pattern. The **pixel electrode** material (5) is formed on the insulating film. **INORGANIC** CHEMISTRY - The drain electrode is formed by material selected from group of iron, cobalt, nickel, chromium, titanium, molybdenum.

USE - For **LCD** device used in OA apparatus, TV, image display device, information terminal.

ADVANTAGE - Improves yield of TFT array substrate by increasing adhesion of wiring and TFT. Improves reliability of TFT array substrate. DESCRIPTION OF DRAWING(S) - The figure shows sectional view showing structure of TFT array substrate. (1) Substrate; (4) Insulation film; (4a) Contact holes; (5) **Pixel electrode**; (10) Adhesion reinforcement agent.

60/3,AB/5 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

05748127
THIN FILM TRANSISTOR ARRAY **SUBSTRATE** AND ITS **MANUFACTURE**

PUB. NO.: 10-031227 [JP 10031227 A]
PUBLISHED: February 03, 1998 (19980203)
INVENTOR(s): MAEDA AKIYOSHI
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 08-184325 [JP 96184325]
FILED: July 15, 1996 (19960715)

ABSTRACT

PROBLEM TO BE SOLVED: To prevent corrosion and to make it possible to secure connection reliability in a connection terminal part by coating a high melting point metallic film arranged in a contact hole inner wall peripheral parts constituting respective connection terminal parts in a buried shape with a gate insulation film and an **inorganic** insulating film.

SOLUTION: A source electrode 22, a drain **electrode** 23, a **pixel electrode** part 15, a signal line and respective connecting terminal parts between scan lines and the signal lines are constituted containing at least the same transparent conductive film 34 as a conductive member. Further, in respective connection terminal parts, the conductive member 34 is constituted so as to be exposed through the contact hole provided on a proper insulation film 33. Then, a high melting point metallic film layer 35 is exposed and arranged on a boundary part between the conductive member 34 and the contact hole inner wall party provided on the insulation film 33 in respective connection terminal parts. Further, the contact hole inner wall part that at least the high melting point metallic film layer 35 is exposed is coated with the **inorganic** insulation film 38.

62/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014160698
WPI Acc No: 2001-644926/200174
XRPX Acc No: N01-482914
Manufacturing method of **bonding substrate** for **liquid crystal display** device used in e.g. notebook PC, involves forming transparent electrode on two substrates, drying and bonding the substrates
Patent Assignee: SHARP KK (SHAF)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2001264734	A	20010926	JP 200078998	A	20000321	200174	B

Priority Applications (No Type Date): JP 200078998 A 20000321
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2001264734	A		10	G02F-001/1333	

Abstract (Basic): JP 2001264734 A
Abstract (Basic):
NOVELTY - Electrically conductive films are formed on **synthetic** resin substrates (1a,2a). The conductive films are then patterned for forming transparent electrodes (1b,2b) on the corresponding substrates (1a,2a). Substrates are then dried in vacuum before exposure, and bonded together.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for **LCD** device manufacturing method.
USE - For **manufacturing bonding substrate** used for **LCD** device used in electronic device e.g. notebook personal computer, palm-top computer, portable information terminal, electronic notebook, mobile telephone.
ADVANTAGE - Alignment accuracy of electrically conductive film pattern between **synthetic** resin substrates is improved.
DESCRIPTION OF DRAWING(S) - The figure shows a sectional view of **LCD** device.
Substrates (1a,2a)
Electrodes (1b,2b)
pp; 10 DwgNo 1/11

65/3,AB/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

00833023
MANUFACTURE OF **LIQUID-CRYSTAL DISPLAY** PANEL

PUB. NO.: 56-153323 [JP 56153323 A]
PUBLISHED: November 27, 1981 (19811127)
INVENTOR(s): NAKAGAWA TETSUO
APPLICANT(s): SEIKO EPSON CORP [000236] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 55-057239 [JP 8057239]
FILED: April 30, 1980 (19800430)
JOURNAL: Section: P, Section No. 104, Vol. 06, No. 34, Pg. 90, March 02, 1982 (19820302)

ABSTRACT

PURPOSE: To obtain a mass-producible orienting **film** having superior **moisture** and heat resistances and strictly contacting with all of glass, a transparent electrode film and a sealant by forming a specified orienting film.

CONSTITUTION: A mixed liquid of at least 1 kind of organosilicic compound such as .gamma.-glycidoxypropyltriethoxysilane having 1-3 hydrolyzable groups and at least 1 kind of **organic** compound of a IVa or IVb group element such as tetraalkoxy type Ge, Sn, Pb, Ti or Zr having 4 hydrolyzable groups is applied to a **liquid crystal display** substrate and calcined to form an orienting film. A cell is **manufactured** using the **substrate** , and after injecting a liquid crystal the cell is sealed. The cell is then exposed to discharge of a gas containing gaseous halogenated hydrocarbon to remove at least the part of the orienting film on the electrode section for a terminal.

69/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013503387
WPI Acc No: 2000-675328/200066
XRAM Acc No: C00-205081
XRPX Acc No: N00-500682

Cleaning of **substrate** used for **manufacture** of electron source **substrate**, involves using cleaning liquid containing chelating reagent, capable of forming insoluble chelate compound with metal ion on substrate

Patent Assignee: CANON KK (CANO)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2000251799	A	20000914	JP 9951221	A	19990226	200066	B

Priority Applications (No Type Date): JP 9951221 A 19990226
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2000251799	A		10	H01J-031/12	

Abstract (Basic): JP 2000251799 A
Abstract (Basic):

NOVELTY - An aqueous cleaning liquid is contacted with a substrate surface used for electronic element formation to elute metal ion adhered on substrate. The cleaning liquid contains a chelating agent capable of forming an insoluble chelate compound with metal ion, in water. The insoluble chelate compound formed after cleaning is then removed.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following: (i) manufacture of electron source board (31). A **conductive film** having electron emission portion on an insulated substrate is provided between a pair of element **electrodes**. The wirings crossing the insulated film are mutually insulated. One of the element **electrode** are connected to wiring along lengthwise direction and other is connected to wiring along crosswise direction; and (ii) image forming apparatus comprising electron source board provided with electron emitting elements and light emission display board. The source and display board are positioned opposite to each other.

USE - For cleaning substrate used for forming functional substrates such as electron source board used in image forming apparatus, **liquid crystal display** device, thin film transistor/ **liquid crystal display** device, plasma display, low speed electron beam fluorescent display tube and cathode ray tube.

ADVANTAGE - Foreign materials such as metal ions (especially lead ions) adhered on the substrate surface can be effectively washed. The image forming apparatus using the functional substrate forms high resolution image.

DESCRIPTION OF DRAWING(S) - The figure shows substrate cleaning method.

69/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013124139
WPI Acc No: 2000-296010/200026
XRAM Acc No: C00-089746
XRPX Acc No: N00-222111
Substrate for plasma display, **LCD**, has dielectric layer and partition layer with predetermined thermal expansion coefficient
Patent Assignee: TORAY IND INC (TORA)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2000063152	A	20000229	JP 98230558	A	19980817	200026	B

Priority Applications (No Type Date): JP 98230558 A 19980817
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2000063152	A		9	C03C-017/04	

Abstract (Basic): JP 2000063152 A
Abstract (Basic):
NOVELTY - A dielectric layer and a partition layer are formed on a glass substrate on which the **electrode** is formed. Thermal expansion coefficient (alpha1) of dielectric layer and thermal expansion coefficient (alpha2) of partition layer at 50-400degreesC satisfies a relation alpha1-alpha2at most10asterisk10-7/K.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for **manufacture** of **substrate**. The dielectric paste containing **inorganic** powder and **organic** component is applied on the glass substrate to form a coating film. Then, the partition paste containing **inorganic** microparticles and photosensitive **organic** component is applied to form a partition pattern by photolithographic method. The coating film and partition pattern are baked simultaneously. The thermal expansion coefficient (alpha1') and thermal expansion coefficient (alpha2') of **inorganic** powder and **inorganic** micro particle at 50-400degreesC satisfies the relation alpha1-alpha2at most10asterisk10-7/K.
USE - For plasma display panel, **liquid crystal display** and image display device using electron-emitting element (claimed).
ADVANTAGE - The generation of curvature and crack on the substrate during formation of dielectric layer and partition layer are prevented. Debonding of dielectric layer and partition layer is prevented. Thus, substrate with highly defined partition is manufactured with sufficient yield.

69/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012712105
WPI Acc No: 1999-518218/199943
XRAM Acc No: C99-151240
XRPX Acc No: N99-385403
Selectively modifying protrusions on a **substrate** for **manufacture** of e.g. a display device
Patent Assignee: MINNESOTA MINING & MFG CO (MINN); 3M INNOVATIVE PROPERTIES CO (MINN)
Inventor: MOSHREFZADEH R S; PADIYATH R; POKORNY R J; WIRTH W M
Number of Countries: 082 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9934256	A1	19990708	WO 98US8995	A	19980504	199943	B
AU 9872812	A	19990719	AU 9872812	A	19980504	199951	
			WO 98US8995	A	19980504		
US 6077560	A	20000620	US 97999287	A	19971229	200035	
EP 1044396	A1	20001018	EP 98920179	A	19980504	200053	
			WO 98US8995	A	19980504		
KR 2001033690	A	20010425	KR 2000707213	A	20000628	200164	
JP 2002500434	W	20020108	WO 98US8995	A	19980504	200206	
			JP 2000526846	A	19980504		

Priority Applications (No Type Date): US 97999287 A 19971229
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9934256	A1	E	27	G03F-007/09	
Designated States (National): AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE GH GM GW HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZW					
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SZ UG ZW					
AU 9872812	A				Based on patent WO 9934256
US 6077560	A			B05D-005/12	
EP 1044396	A1	E		G03F-007/09	Based on patent WO 9934256
Designated States (Regional): BE DE DK FR GB IT NL					
KR 2001033690	A			G03F-007/09	
JP 2002500434	W		24	H01L-021/304	Based on patent WO 9934256

Abstract (Basic): WO 9934256 A1
Abstract (Basic):

NOVELTY - Protrusions on a substrate are selectively modified by coating the surface with a planarizing filler, exposing the tops of the protrusions and modifying by e.g. depositing a metal.

DETAILED DESCRIPTION - Protrusions on a structured substrate are selectively modified by: coating the surface with a filler which covers the protrusions; planarizing the filler surface; removing the filler uniformly to expose the protrusions; and modifying the exposed surfaces of the protrusions. Preferably the protrusions are parallel ridges of equal height and separation less than 1000 micron and height less than

50 micron. The modification step preferably comprises removing a transparent **conductive** oxide, preferably indium tin oxide, from the exposed surfaces, or depositing a material, preferably a metal, on the exposed surfaces.

USE - In manufacture of **liquid crystal display** substrates, high definition large-screen television displays etc.

ADVANTAGE - Maskless patterning of substrate structures is achieved in a continuous process independent of the substrate and pattern dimensions.

DESCRIPTION OF DRAWING(S) - The drawing shows a substrate with structural elements at the initial stage of the process of the invention

Substrate (10)

Protrusions, preferably parallel ridges (12)

Filler material, preferably a photoresist, flooding the substrate and covering the protrusions by a thickness d (20)

pp; 27 DwgNo 1a/2

69/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012067836
WPI Acc No: 1998-484747/199842
XRPX Acc No: N98-378292
Substrate manufacturing method for **LCD** panel - involves shifting edge of **organic** orientation film from that of insulating film by 0.5-1mm
Patent Assignee: MATSUSHITA DENKI SANGYO KK (MATU)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 10206855	A	19980807	JP 9711774	A	19970127	199842	B

Priority Applications (No Type Date): JP 9711774 A 19970127
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 10206855	A		4	G02F-001/1337	

Abstract (Basic): JP 10206855 A

The method involves forming a transparent **electrode** (3) on the surface of a glass substrate. An **inorganic** insulating film (4) and an **organic** orientation film (5) are laminated on the transparent **electrode**.

The edge of the **organic** orientation film is shifted from the edge of the insulating film by 0.5-1mm. The rubbing of the orientation film is carried out by the rubbing roller (6).

ADVANTAGE - Facilitates uniform rubbing of orientation film. Improves display quality of panel.

69/3,AB/5 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

05809990
SEMICONDUCTOR DEVICE, ITS **MANUFACTURE**, AND **ORGANIC** RESIN **SUBSTRATE** FOR SEMICONDUCTOR DEVICE

PUB. NO.: 10-093090 [JP 10093090 A]
PUBLISHED: April 10, 1998 (19980410)
INVENTOR(s): YAMADA HIROSAKU
KIYOTA TOSHIYA
UCHIKOGA SHIYUUICHI
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 08-242785 [JP 96242785]
FILED: September 13, 1996 (19960913)

ABSTRACT

PROBLEM TO BE SOLVED: To enable forming a coating, having a sufficient barrierability, even if a general resin material is used, by forming a semiconductor film in which an active layer for a semiconductor device has been formed, on an **inorganic** insulating film containing specified impurities on an **organic** resin substrate.

SOLUTION: An acrylic resin substrate containing Na being an alkaline metal of a sufficient concentration is used. First, SiO(sub 2) 2 of 30nm is deposited on a substrate 1 by 100 deg.C plasma CVD, using SiH(sub 4) and N(sub 2)O as materials. The formation condition is 120 deg.C. Following this, this substrate 1 is dipped in a 5% NaCl aqueous solution 3, put in a glass container 5 for 48 hours, is washed simply after that, and is dried subsequently to form a plastic substrate sufficiently polluted by Na. An SiO(sub 2) film 4 is deposited by 200nm with CVD, similarly to the SiO(sub 2) 2 forming process. Next, As ions are used and implanted to a specified concentration with an acceleration energy of 40keV, it is possible to obtain a blocking ability with respect to alkaline metals by this coating

69/3,AB/6 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

03599016
MANUFACTURE OF LIQUID CRYSTAL ELECTROOPTIC DEVICE

PUB. NO.: 03-261916 [JP 3261916 A]
PUBLISHED: November 21, 1991 (19911121)
INVENTOR(s): YAMAZAKI SHUNPEI
APPLICANT(s): SEMICONDUCTOR ENERGY LAB CO LTD [470730] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 02-062019 [JP 9062019]
FILED: March 13, 1990 (19900313)
JOURNAL: Section: P, Section No. 1314, Vol. 16, No. 68, Pg. 116, February 19, 1992 (19920219)

ABSTRACT

PURPOSE: To reduce the weight of the liquid crystal electrooptic device and to suppress a decrease in the yield by forming **organic** or **inorganic** thin films on **electrode manufacture** surfaces of two **substrates** , sticking the two substrates together and injecting liquid crystal between the substrates, and connecting a semiconductor integrated circuit chip for liquid crystal driving to an **electrode**.

CONSTITUTION: **Conductive films** are formed on the substrates 1 and 5 and cut by being irradiated with laser light to manufacture **electrodes** 2 and 6, and the **organic** or **inorganic** thin films 4 and 7 for orienting the liquid crystal 9 are formed on the **electrode manufacture** surfaces of the **substrates** 1 and 5.

Then 1st and 2nd substrates 2 and 5 are stuck, the liquid crystal 9 is injected between the 1st and 2nd substrates, and die bonding is carried out for the semiconductor integrated circuit for driving the liquid crystal. Further, the connection pad of the semiconductor integrated circuit chip 11 and the **electrode** formed on the 1st or 2nd substrate are connected by wire bonding 13. Consequently, the liquid crystal electrooptic device is reduced in weight, the decrease in the yield is eliminated, and a rise in the cost is suppressed.

69/3,AB/7 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO

01304321
MANUFACTURE OF **SUBSTRATE** FOR HOLDING LIQUID CRYSTAL

PUB. NO.: 59-015921 [JP 59015921 A]
PUBLISHED: January 27, 1984 (19840127)
INVENTOR(s): YAMAZAKI MITSUO
UCHIMURA SHUNICHIRO
SATO TONOBU
MAKINO DAISUKE
UCHIGASAKI ISAO
APPLICANT(s): HITACHI CHEM CO LTD [000445] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 57-126601 [JP 82126601]
FILED: July 19, 1982 (19820719)
JOURNAL: Section: P, Section No. 274, Vol. 08, No. 105, Pg. 89, May 17, 1984 (19840517)

ABSTRACT

PURPOSE: To enable **liquid crystal display** of high quality by applying a composition containing specified polyamic acid to the liquid crystal sides of substrates each having a transparent **electrode** film, and causing the ring closure of the polyamic acid by dehydration to form polyimide films.

CONSTITUTION: Biphenyltetracarboxylic acid anhydride is brought into reaction with diamine such as m-phenylenediamine in a solvent to produce polyamic acid. The resulting composition containing polyamic acid is applied to the liquid crystal sides of substrates each having a transparent **electrode** film, and by heating the substrates, the ring closure of the polyamic acid is caused by dehydration to form polyimide films. Thus, the desired substrates for holding a liquid crystal are obtained The polyimide films used as orienting films are slightly colored, and they have superior adhesive properties to the substrates and superior orientation controlling power for keeping a liquid crystal in a homogeneously oriented state. The orientation controlling power is not deprived by heat treatment.

69/3,AB/8 (Item 4 from file: 347)
DIALOG(R)File 347:JAPIO

01101526
MANUFACTURE OF TRANSPARENT RESIN **SUBSTRATE** OF **LIQUID CRYSTAL DISPLAY** DEVICE

PUB. NO.: 58-038926 [JP 58038926 A]
PUBLISHED: March 07, 1983 (19830307)
INVENTOR(s): MASAKI YUTAKA
SAITO TETSUO
APPLICANT(s): CANON INC [000100] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 56-137505 [JP 81137505]
FILED: September 01, 1981 (19810901)
JOURNAL: Section: P, Section No. 199, Vol. 07, No. 121, Pg. 71, May 25, 1983 (19830525)

ABSTRACT

PURPOSE: To manufacture continuously and easily a transparent resin substrate having a uniform orienting film by continuously moving a beltlike film substrate and forming a resin film on the moving substrate by a roll coating method or a spraying method using a resin solution for forming an orienting film or an orienting agent.

CONSTITUTION: In the figure 5' is a coil of a polyethylene terephthalate film 5 having a required transparent **electrode** film on the surface. The film 5 is continuously moved by means of guide rolls as shown by the figure, and it is coiled. While moving the film 5, methyl-.gamma.-aminopropyltrimethoxysilane as an orienting agent is applied to the film 5 by means of a roll coater 6. The film 5 is optionally heated to about 100c with a heater 7 and dried to adhere the orienting agent to the substrate, and the film 5 is continuously coiled to form a coil 5''.

69/3,AB/9 (Item 5 from file: 347)
DIALOG(R)File 347:JAPIO

00863126
LIQUID CRYSTAL DISPLAY ELEMENT

PUB. NO.: 57-013426 [JP 57013426 A]
PUBLISHED: January 23, 1982 (19820123)
INVENTOR(s): TAKANASHI HIROSHI
APPLICANT(s): SHARP CORP [000504] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 55-087362 [JP 8087362]
FILED: June 26, 1980 (19800626)
JOURNAL: Section: P, Section No. 114, Vol. 06, No. 75, Pg. 106, May 12, 1982 (19820512)

ABSTRACT
PURPOSE: To simply prevent the occurrence of a defective display in a **liquid crystal display** element having a structure with **organic** orienting films by forming a film of an **organic** substance such as silicon modified polyimide between each of the orienting films and a substrate and between an **organic** sealant and the substrate.
CONSTITUTION: **Organic** orienting **film** 5, electrically **conductive films** 3 and **inorganic** insulating films 2 are laminated on the upper and lower sides of a liquid crystal material 7 in succession, and they are sealed with substrates 1 and an **organic** sealant 6. At this time, a heat resistant coupling film 10 is interposed between each of the films 5 and each of the **substrates** 1 to **manufacture** the desired **liquid crystal display** element. The film 10 is formed in about 10 angstroms thickness using silicone modified polyimide such as polyimidosiloxane, silicone modified urethane or other **organic** coupling agent. Thus, a **liquid crystal display** device orienting liquid crystal molecules uniformly and having high display quality can be obtained

69/3,AB/11 (Item 7 from file: 347)
DIALOG(R)File 347:JAPIO

00666318
LIQUID CRYSTAL DISPLAY CELL AND ITS PRODUCTION

PUB. NO.: 55-153918 [JP 55153918 A]
PUBLISHED: December 01, 1980 (19801201)
INVENTOR(s): AOKI TOSHIHIRO
APPLICANT(s): CASIO COMPUT CO LTD [350750] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 54-061168 [JP 7961168]
FILED: May 18, 1979 (19790518)
JOURNAL: Section: P, Section No. 49, Vol. 05, No. 26, Pg. 158, February 17, 1981 (19810217)

ABSTRACT

PURPOSE: To enable the fusion-superposition of substrates without losing the orientation characteristic of orientation films by forming an insulation layer composed of **inorganic** material between the substrate surface of an **electrode** substrate formed with an orientation film composed of **organic** material and the **electrodes**.

CONSTITUTION: An insulation layer 3 such as SiO(sub 2) is formed over the entire top surface of a glass substrate 1a by a sputtering method or the like and transparent **electrodes** 5 are formed on the insulation layer 3. Thence, an orientation film 7 of **organic** material such as polyimide is formed by coating on the **electrode**-formed surface and the surface of the orientation film 7 is lapped to **manufacture** the **electrode substrate** 1. An **electrode substrate** 2 is **manufactured** in a similar manner. To assemble the **liquid crystal display** cell, the foregoing two **electrode** substrates 1, 2 assuming a pair are opposed by leaving a liquid crystal sealing spacing and are fusion-superposed at fusion-bonding temperatures 400-500 deg.C by frit glass.

73/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014376624
WPI Acc No: 2002-197327/200226
XRPX Acc No: N02-149896
Self-light emitting device used for electrical appliances such as portable game machine, has electroluminescent element covered with **inorganic** material film which is further covered with organic material film
Patent Assignee: SEMICONDUCTOR ENERGY LAB (SEME); SEL SEMICONDUCTOR ENERGY LAB (SEME)
Inventor: NORIKO I; SHUNPEI Y
Number of Countries: 029 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 1139453	A2	20011004	EP 2001107616	A	20010327	200226	B
CN 1320971	A	20011107	CN 2001117396	A	20010327	200226	
JP 2001345174	A	20011214	JP 200187851	A	20010326	200226	
KR 2001098431	A	20011108	KR 200116006	A	20010327	200227	

Priority Applications (No Type Date): JP 200087355 A 20000327
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 1139453	A2	E	38	H01L-051/20	
Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR					
CN 1320971	A			H01L-033/00	
JP 2001345174	A		21	H05B-033/04	
KR 2001098431	A			H05B-033/04	

Abstract (Basic): EP 1139453 A2
Abstract (Basic):
NOVELTY - The self-light emitting device has an electroluminescent (EL) element covered or contacted with an **inorganic** material film which is covered with an organic material film. Alternately, the device has an EL element covered or contacted with an organic material film which is covered with an **inorganic** material film.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:
(a) Electric appliance using self-light emitting device; and
(b) Method of manufacturing self-light emitting device
USE - For electrical appliances (claimed) such as video camera, digital camera, goggles-type display (head mount display), navigation system, sound reproduction device (car audio equipment and audio set), note-size personal computer, game machine, portable information terminal (mobile computer, portable telephone, portable game machine, electronic book), and image reproduction apparatus including recording medium such as digital video disk (DVD).
ADVANTAGE - The electroluminescent display is of self-emission type and therefore requires no back light. The display portion has a thickness thinner than that of liquid crystal display device. The

self-emission device exhibits high response speed. The cover **layer** has **moisture** absorbing effect which prevents penetration of moisture inside the element. The barrier and cover layers completely cut off the EL element from external environment and invasion from moisture and oxygen which accelerate the oxidative degradation of EL layer. The provision of cover layer is effective for the stress relaxation of **thin film transistor** or EL element.

76/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014409076
WPI Acc No: 2002-229779/200229
XRAM Acc No: C02-069860
XRPX Acc No: N02-176747
Polyimide silicone resin for forming film on electronic components or semiconductor devices, is derived from diamine comprising diaminopolysiloxane and acid dianhydride, and exhibits preset properties
Patent Assignee: SHINETSU CHEM CO LTD (SHIE); SHINETSU CHEM IND CO LTD (SHIE); KATO H (KATO-I); SUGO M (SUGO-I)
Inventor: KATO H; SUGO M
Number of Countries: 029 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 1167423	A2	20020102	EP 2001115362	A	20010626	200229	B
JP 2002012667	A	20020115	JP 2000196843	A	20000629	200229	
US 20020016408	A1	20020207	US 2001892445	A	20010628	200229	
KR 2002002306	A	20020109	KR 200138095	A	20010629	200246	

Priority Applications (No Type Date): JP 2000196843 A 20000629
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 1167423	A2	E	9	C08G-077/455	
Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR					
JP 2002012667	A		7	C08G-077/455	
US 20020016408	A1			C08J-003/00	
KR 2002002306	A			C08G-077/455	

Abstract (Basic): EP 1167423 A2
Abstract (Basic):
NOVELTY - A polyimide silicone resin, is derived from a diamine comprising a diaminopolysiloxane and an acid dianhydride. The resin comprises at least 50 weight% (wt.%) of siloxane residual group, and has an elongation at rapture (sic) of 400% or higher, and a modulus of elasticity of 500 N/mm2 or less.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(i) a polyimide silicone resin solution composition comprising polyimide silicone resin and an **organic** solvent capable of dissolving the resin; and

(ii) a polyimide silicone resin film comprising polyimide silicone resin formed on a substrate.

USE - The method is used for forming polyimide silicone resin film such as electrode protective **film** or **moisture proof** protective **film** on electronic component parts, liquid crystal display panels or semiconductor devices. The method is used for forming electrode protective film for **thin film transistor** (**TFT**) liquid crystal display panels, super twisted nematic (STN) liquid crystal display panels or plasma display panels, as junction

films for integrated circuits and as conformal coating of printed circuit boards.

ADVANTAGE - The silicone resin forms films at relatively low temperature, has superior adhesiveness to the substrate, durability under conditions of high humidity, and low stress and high elongation. The solution composition forms resin film with ease. The resin film obtained from the resin composition, causes neither warpage nor copper sheet corrosion when applied on glass sheets or copper sheets.

pp; 9 DwgNo 0/0

76/3,AB/2 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

06635674

LIQUID CRYSTAL DISPLAY DEVICE

PUB. NO.: 2000-221488 [JP 2000221488 A]
PUBLISHED: August 11, 2000 (20000811)
INVENTOR(s): MURAI ATSUTO
OKADA YOSHIHIRO
BAN ATSUSHI
APPLICANT(s): SHARP CORP
APPL. NO.: 11-021047 [JP 9921047]
FILED: January 29, 1999 (19990129)

ABSTRACT

PROBLEM TO BE SOLVED: To inhibit the polarization of an interlayer insulating film remarkably caused when voltage is applied to **TFT** and the generation of electric charges on the surface of an a-Si layer due to the polarization and to inhibit the deterioration of the characteristics of **TFT** by incorporating water absorbing particles or moisture adsorbing particles into the interlayer insulating film.

SOLUTION: A photosensitive **organic** material mixed with water absorbing particles or moisture adsorbing particles 13 is used for an interlayer insulating **film** 9. Since **moisture** in the interlayer insulating film 9 is adsorbed or absorbed, the polarization of the interlayer insulating film 9 remarkably caused when voltage is applied to **TFT** during the rise of the concentration of **moisture** in the **film** 9 and the generation of electric charges on the surface of an a-Si layer 5 due to the polarization are inhibited and the deterioration of the characteristics of **TFT** after panel aging is inhibited. Since dry etching time can therefore be shortened, the thickness of the interlayer insulating film 9 is hardly reduced, uniformity in thickness reduction in the surface of a substrate is enhanced and the occurrence of unevenness in display in panel display can be prevented.

76/3,AB/3 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

04586763
LIQUID CRYSTAL DISPLAY SUBSTRATE

PUB. NO.: 06-258663 [JP 6258663 A]
PUBLISHED: September 16, 1994 (19940916)
INVENTOR(s): HIROSHIMA MINORU
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 05-042422 [JP 9342422]
FILED: March 03, 1993 (19930303)
JOURNAL: Section: P, Section No. 1842, Vol. 18, No. 657, Pg. 56, December 13, 1994 (19941213)

ABSTRACT

PURPOSE: To prevent the seizure in image display by setting the protective film formed on electrodes provided on a liquid crystal display substrate surface on the side in contact with a liquid crystal at a specific range.

CONSTITUTION: A **thin-film transistor TFT** and a transparent pixel electrode ITO1 are provided thereon with the protective film PSV1. The protective film PSV1 is formed mainly to protect the **TFT** against **moisture** and a **film** having good **moisture** resistance is used. The protective film PSV1 consists of an **organic** resin film and is formed by spin coating or printing. Conductive particulates are scattered in this **organic** resin film and, therefore, the specific resistance .rho.of the protective film PSV1 is set at 10(sup 9) to 10(sup 13).omega..cm. The protective film has a middle insulating characteristic. The protective film PSV1 has the middle insulating characteristic like this and, therefore, even if charges remain in this insulating film, the remaining time thereof is shortened. Consequently, the influence acting on the next displayed image is lessened.

80/3,AB/2 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

06847345
SEMICONDUCTOR DEVICE AND RADIATION IMAGING SYSTEM USING THE DEVICE

PUB. NO.: 2001-074845 [JP 2001074845 A]
PUBLISHED: March 23, 2001 (20010323)
INVENTOR(s): OKADA SATOSHI
MOCHIZUKI CHIORI
MORISHITA MASAKAZU
APPLICANT(s): CANON INC
APPL. NO.: 11-250295 [JP 99250295]
FILED: September 03, 1999 (19990903)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a semiconductor device whose breakdown is prevented in a pasting operation and whose light receiving sensitivity is enhanced by forming a protective layer which covers a scintillator.

SOLUTION: First, aluminum is vapor-deposited on a baseplate 117. A reflecting layer 116 is formed. A mask 132 is vapor-deposited on its end part so as to be mounted inside a vacuum chamber. Cesium iodide is vapor-deposited on a required part on the reflected layer 116. A scintillator 115 is formed. Then, a **moisture** protective **layer** 114 is formed on it, and the baseplate is completed. On the other hand, a MIS-type photosensor part 102, a **TFT** switching part 103 and an **electrode** part 104 are formed on a glass substrate 101. A first protective layer 111 is formed on it. In addition, a second protective layer is formed on it, and it is cut to a design size. An adhesive layer 113 is coated on the second protective layer so as to be pasted on the scintillator 115. Then, lastly, a sealing agent 121 is applied.

80/3,AB/3 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

06332907
THIN FILM TRANSISTOR AND LIQUID CRYSTAL DISPLAY

PUB. NO.: 11-274509 [JP 11274509 A]
PUBLISHED: October 08, 1999 (19991008)
INVENTOR(s): HIRAI KYOKO
JINNO MASASHI
APPLICANT(s): SANYO ELECTRIC CO LTD
APPL. NO.: 10-078771 [JP 9878771]
FILED: March 26, 1998 (19980326)

ABSTRACT

PROBLEM TO BE SOLVED: To provide an FET and a liquid crystal display(LCD) with few detects and uniform illumination in plane, by reducing a change in threshold voltage when polarization of a flattened film or an interlayer **film** is caused by **moisture** or impurity ions in **thin film transistor**(FET).

SOLUTION: In a **thin film transistor**, a gate **electrode** 2, a gate insulating film, a polycrystal silicon film, a stopper insulating film on the channel 7, an interlayer film 12, a source **electrode** 5, a drain **electrode** 6, a flattened film 15, and a transparent **electrode** are formed sequentially. One of the source **electrode** 5 and the drain **electrode** 6 is formed on the interlayer film 12 in a way that an upper part of the channel 7 is covered with the **electrode**.

80/3,AB/4 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO

05692316
INSULATED-GATE TYPE FIELD-EFFECT SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

PUB. NO.: 09-307116 [JP 9307116 A]
PUBLISHED: November 28, 1997 (19971128)
INVENTOR(s): MOROSAWA NARIHIRO
APPLICANT(s): SHARP CORP [000504] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 08-124480 [JP 96124480]
FILED: May 20, 1996 (19960520)

ABSTRACT

PROBLEM TO BE SOLVED: To make it possible to form a dense and high-quality gate insulating **film**, wile adsorbs little **moisture**, at a low temperature in a later process by a method wherein a semiconductor film, a gate insulating film and a gate **electrode** are stacked on the insulative substrate in this order, from the substrate side and the gate insulating film is made of an F atom-containing SiO(sub 2) layer.

SOLUTION: First, a semiconductor film 2 is formed on an insulative substrate 1. Then, an F atom-containing SiO(sub 2) film 3, which is used as a gate insulating film, is formed on this film 2. Then, a gate **electrode** 4 is formed on the gate insulating film 3. Then, the surface of the **electrode** 4 is anodized to form an anodized film 5. Subsequently, the film 2 is doped in a self alignment manner using the **electrode** 4 and the film 5 as masks to form a source region 6 and a drain region 6. After that, an interlayer insulating film 7 is formed in such a way as to cover the **electrode** 4 and the film 5. Then, contact holes are formed and lead-out **electrodes** 8 are formed on the film 7 to complete a **TFT**.

80/3,AB/5 (Item 4 from file: 347)
DIALOG(R)File 347:JAPIO

04786397
FABRICATION OF SUBSTRATE FOR DISPLAY ELEMENT

PUB. NO.: 07-078997 [JP 7078997 A]
PUBLISHED: March 20, 1995 (19950320)
INVENTOR(s): IWANAGA TOSHIHIKO
INO MASUMITSU
KAISE KIKUO
URAZONO TAKENOBU
IKEDA HIROYUKI
APPLICANT(s): SONY CORP [000218] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 06-079410 [JP 9479410]
FILED: March 24, 1994 (19940324)

ABSTRACT

PURPOSE: To reduce fabrication cost by depositing a cap film for blocking diffusion of hydrogen on a interlayer **film**, thermally decomposing the **moisture** captured by the interlayer film to generate hydrogen, and then introducing the hydrogen to a polycrystalline semiconductor thin film.

CONSTITUTION: A gate oxide 3 is deposited on the surface of a polycrystalline semiconductor thin film 2 formed on a glass substrate 1 and a gate **electrode** G is disposed thereon to obtain a **TFT** 4. A dielectric and hygroscopic interlayer film 5 is then deposited and etched to make a contact hole opening to a source region S. Subsequently, a cap film 6 for blocking diffusion of hydrogen is deposited on the interlayer **film** 5. **Moisture** captured by the interlayer film 5 is thermally decomposed to generate hydrogen which is then introduced to the polycrystalline semiconductor film 2. The cap film 3 is then patterned into a wiring **electrode** for the source region S and an interlayer film 7 is deposited. Subsequently, the interlayer films 5, 7 are etched to make a contact hole to the drain region D and then a pixel **electrode** 8 is formed on the interlayer film 7.

80/3,AB/6 (Item 5 from file: 347)
DIALOG(R)File 347:JAPIO

04251572
MANUFACTURE OF **THIN-FILM TRANSISTOR**

PUB. NO.: 05-243272 [JP 5243272 A]
PUBLISHED: September 21, 1993 (19930921)
INVENTOR(s): OKA HITOSHI
EMOTO FUMIAKI
NAKAMURA AKIRA
SENDA KOJI
ISHIHARA TOMOAKI
APPLICANT(s): MATSUSHITA ELECTRON CORP [000584] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 04-044470 [JP 9244470]
FILED: March 02, 1992 (19920302)
JOURNAL: Section: E, Section No. 1482, Vol. 17, No. 702, Pg. 89, December 21, 1993 (19931221)

ABSTRACT

PURPOSE: To reduce the unevenness on a metal wiring and improve the resistance to **moisture** of a **thin-film transistor** for applying to a video display device of active matrix type used for a view finder of a video tape recorder, a projection television, a compact television receiver or the like.

CONSTITUTION: A polycrystalline silicon thin film 2, a gate insulating film 3 and a gate **electrode** 4 are sequentially formed on the surface of an insulator substrate 1. Then, an impurity is ion-implanted, and source and drain regions 11 are formed. A **thin film transistor** 10 is formed and an interlayer insulating film 5 is formed on the **thin film transistor** 10. After a sintering is performed with hydrogen gases, a metal wiring 6 is formed and finally a passivation film 7 is formed. By such construction, the unevenness on the metal wiring 6 can be reduced and the resistance to **moisture** of the **thin film transistor** 10 can be improved.

80/3,AB/7 (Item 6 from file: 347)
DIALOG(R)File 347:JAPIO

02691474
SOLID-STATE IMAGE SENSING DEVICE

PUB. NO.: 63-308374 [JP 63308374 A]
PUBLISHED: December 15, 1988 (19881215)
INVENTOR(s): IWAMOTO KOICHI
APPLICANT(s): SEIKO EPSON CORP [000236] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 62-144873 [JP 87144873]
FILED: June 10, 1987 (19870610)
JOURNAL: Section: E, Section No. 741, Vol. 13, No. 147, Pg. 65, April 11, 1989 (19890411)

ABSTRACT

PURPOSE: To make it possible to obtain both excellent tight adhesiveness and a **moisture-proof** property by a method wherein a passivation layer, consisting of a first layer of silicon dioxide (SiO(sub 2)) film and a second layer of the SiO(sub 2) film which is formed more densely than the first layer, are formed by a sputtering method.

CONSTITUTION: In the solid-state image sensing device consisting of the photodetector which is formed by providing amorphous silicon on an insulative substrate 1 and the **thin film transistor** which drives the photosensor, an SiO(sub 3) film 9 is formed as the first layer, and a passivation layer 10 consisting of the SiO(sub 2) film, which is formed more densely than the first layer, is formed as the second **layer** by **conducting** a sputtering method. As a result, excellent tight adhesive property can be obtained, the film quality of passivation film can be stabilized, a moisture blocking function can be displayed sufficiently, and the reliability in **moisture-proof** property can also be improved.

08/02/2002 09/808,957

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File 348:EUROPEAN PATENTS 1978-2002/Jul W03
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File 349:PCT FULLTEXT 1983-2002/UB=20020801,UT=20020725
(c) 2002 WIPO/Univentio

Set	Items	Description
S1	1469	((THIN()FILM()TRANSISTOR) OR TFT)/TI,AB,CM
S2	9098	(LCD OR (LIQUID()CRYSTAL()DISPLAY? ?))/TI,AB,CM
S3	1318	(MANUFACT??????(3N)SUBSTRATE? ?)/TI,AB,CM
S4	12	(MANUFACT??????(3N)SUBSTRATE? ?(3N)(INORGANIC?????? OR ARTIFICIAL? ? OR SYNTHETIC??????))/TI,AB,CM
S5	70096	((INORGANIC?????? OR ARTIFICIAL? ? OR SYNTHETIC??????))/TI,AB,CM
S6	70096	S4:S5
S7	1306	(PRODUCT? ?(3N)SUBSTRATE? ?)/TI,AB,CM
S8	12	(PRODUCT? ?(3N)(SUBSTRATE(3N)ORGANIC??????))/TI,AB,CM
S9	80030	(ORGANIC??????)/TI,AB,CM
S10	80030	S8:S9
S11	246	((BOND?????? OR JOIN??????)()SUBSTRATE? ?)/TI,AB,CM
S12	296	(MOISTUR??????(3N)PROOF)/TI,AB,CM
S13	1601	(MOISTUR??????(3N)(LAYER??? OR FILM??? OR COAT??? OR MULTILAYER??? OR SPACER???))/TI,AB,CM
S14	1818	S12:S13
S15	1296	(PIXEL? ?(3N)(ELECTRODE? ? OR MICROELECTRODE? ? OR CONDUCT????))/TI,AB,CM
S16	195539	(ELECTRODE? ? OR MICROELECTRODE? ? OR CONDUCT????)/TI,AB,CM
S17	23802	((CONDUCT??????)(3N)(LAYER??? OR FILM??? OR COAT??? OR MULTILAYER??? OR SPACER???))/TI,AB,CM
S18	196068	S16:S17
S19	556	((ELECTRO()LUMINESCEN?????? OR ELECTROLUMINESCEN??????)(3N)(DISPLAY?????? OR SCREEN? ?))/TI,AB,CM
S20	523	S1 AND S2
S21	13	S20 AND S3
S22	2	S21 AND S6
S23	11	S21 NOT S22
S24	0	S23 AND S7
S25	1	S23 AND S10
S26	10	S23 NOT S25
S27	0	S26 AND S11
S28	0	S26 AND S14
S29	4	S26 AND S15
S30	4	IDPAT (sorted in duplicate/non-duplicate order)
S31	4	IDPAT (primary/non-duplicate records only)
S32	6	S26 NOT S31
S33	6	IDPAT (sorted in duplicate/non-duplicate order)
S34	6	IDPAT (primary/non-duplicate records only)
S35	392	S20 AND S18
S36	179	S35 AND S15
S37	2	S36 AND S19
S38	177	S36 NOT S37
S39	0	S38 AND S14
S40	16	S38 AND S10
S41	3	S40 AND S6
S42	13	S40 NOT S41
S43	13	S42 AND S2
S44	1	S42 AND S3
S45	12	S43 NOT S44
S46	0	S45 AND S14

S47	0	S20 AND S14
S48	3	S1 AND S14
S49	7	S2 AND S14
S50	7	IDPAT (sorted in duplicate/non-duplicate order)
S51	6	IDPAT (primary/non-duplicate records only)
S52	6	S51 NOT S48
S53	81	S1 AND (S3 OR S6)
S54	33	S53 AND (S7 OR S10)
S55	0	S54 AND S11
S56	11	S54 AND S15
S57	11	S56 AND S18
S58	1	S56 AND S19
S59	11	IDPAT S57 (sorted in duplicate/non-duplicate order)
S60	11	IDPAT S57 (primary/non-duplicate records only)
S61	13	S20 AND S19
S62	1	S61 AND S6

22/TI,PD,PY,PN,K/1 (Item 1 from file: 348)

TFT ARRAY **SUBSTRATE**, METHOD OF **MANUFACTURE** THEREOF, AND **LCD** WITH **TFT** ARRAY SUBSTRATE
TFT-FELD-SUBSTRAT, VERFAHREN ZU DESSEN HERSTELLUNG, UND **LCD** MIT **TFT**-FELD-SUBSTRAT
SUBSTRAT TABLEAU A MATRICE ACTIVE, PROCEDE DE FABRICATION, ET AFFICHEUR A CRISTAUX LIQUIDES MUNI D'UN SUBSTRAT TABLEAU A MATRICE ACTIVE
PATENT (CC, No, Kind, Date): EP 1168054 A1 020102 (Basic)
WO 200148547 010705

A structure for a **TFT** array substrate is provided, that can be produced using only two or three photomasks. This can be achieved with a **TFT** array substrate including pixel electrodes (14') and TFTs (16) including a silicon semiconductor film deposited over the insulating substrate (1), a gate insulator film (4...
substrate (1).

18. A **liquid crystal display** device, comprising:
a first substrate, wherein a liquid crystal alignment film is formed on a surface of a top gate **TFT** array substrate, wherein pixel electrodes and TFTs driving the pixel electrodes are arranged in a matrix on an insulating substrate; and
a second substrate including...

19. The **liquid crystal display** device according to claim 18, wherein the TFTs (16) and the pixel electrodes (14') on the top gate **TFT** array substrate are covered with a protective film.

20. The **liquid crystal display** device according to claim 19, wherein the protective film is made of an **inorganic** material.

21. A method for manufacturing a **liquid crystal display** device, comprising:
a **TFT** array **substrate manufacturing** process for **manufacturing** a top gate **TFT** array substrate including:
a group of TFTs comprising:
a silicon semiconductor film deposited over an insulating substrate (1);

a gate insulator film (4') formed over...semiconductor film via the drain electrode (13);
an alignment film formation process, wherein a liquid crystal alignment film is formed on a surface of the **TFT** array substrate to make a first substrate; and
a device assembly process, wherein a **liquid crystal display** device is made by superposing the first substrate and a second substrate, which includes a color filter group and an opposing electrode, with their electrode surfaces facing inward, and injecting a liquid crystal into a gap between the two substrates;

wherein the **TFT** array **substrate manufacturing** process comprises:
a first layering step, wherein an intrinsic silicon semiconductor film layer (3) not doped with impurities, a gate insulator film layer (4), and...

44. A method for manufacturing a **liquid crystal display** device, comprising:
a reflective **TFT** array **substrate manufacturing** process for **manufacturing** a reflective **TFT** array substrate including:
a silicon semiconductor film deposited over an insulating substrate (1);

22/TI,PD,PY,PN,K/2 (Item 1 from file: 349)

ACTIVE MATRIX SUBSTRATE FOR **LIQUID CRYSTAL DISPLAY** AND METHOD OF MANUFACTURE FOR MAKING THE SAME
SUBSTRAT DE MATRICE ACTIVE POUR AFFICHAGE A CRISTAUX LIQUIDES ET PROCEDE DE FABRICATION DE CEUX-CI

Patent and Priority Information (Country, Number, Date):
Patent: WO 200140856 A1 20010607 (WO 0140856)
Publication Year: 2001

English Abstract
A transistor substrate for a **liquid crystal display** comprises an array of insulated-gate staggered TFTs and a capacitor (36) associated with each transistor. The gate insulator (400,420) comprises a first **inorganic** layer (400) and a second, polymer or spin-on glass layer (420), of which layers only the polymer or spin-on glass layer (420) extends...

1 . A transistor. substrate for a **liquid crystal display** comprising: a substrate; a transistor over the substrate, the transistor comprising an insulated-gate staggered structure having substantially coplanar source and drain regions and a...

...adjacent the transistor, the capacitor comprising a stacked structure of two electrodes separated by a capacitor dielectric, wherein the io gate insulator comprises a first **inorganic** layer and a second, polymer or spinon glass layer, of which layers only the polymer or spin-on glass layer extends to the capacitor to...

8 A display as claimed in claim 6 or 7, wherein the first layer comprises an **inorganic** layer, and the second layer comprises a polymer or spin-on glass layer.
. A display as claimed in claim 8, wherein the second layer comprises polyimide.

10 A method of **manufacturing** a transistor **substrate** for a **liquid crystal display**, comprising: providing an array of transistors and capacitors over the substrate, the transistors comprising insulated-gate staggered structures having substantially coplanar source and drain regions...

...the capacitors, and the second layer extending to the areas corresponding to the capacitors to define the capacitor dielectric.

11 A method of manufacturing a **liquid crystal display**, comprising **manufacturing** a transistor **substrate** using the method of claim 8, and

31/TI,PD,PY,PN,K/1 (Item 1 from file: 348)

Analyzing method and apparatus for minute foreign substances, and manufacturing methods for manufacturing semiconductor device and **liquid crystal display** device

Verfahren und Gerat zur Analyse von winzigen Fremdkorpern und Herstellungsverfahren von Halbleiter- und **LCD**-Vorrichtungen unter Anwendung desselben

Procede et appareil d'analyse d'impuretes minuscules, et procedes de fabrication de dispositifs semiconducteurs et de panneaux a cristaux liquides l'utilisant

PATENT (CC, No, Kind, Date): EP 727660 A2 960821 (Basic)
EP 727660 A3 980304

10. An analyzing method as set forth in claim 7, 8 or 9, wherein the angular substrate is a **liquid crystal display** element midway during a manufacturing process for manufacturing a **liquid crystal display** device, or an insulative transparent substrate from which the **liquid crystal display** element is being manufactured.
11. An analyzing apparatus for analyzing foreign substances, the analyzing apparatus for analyzing foreign substances comprising a stage on which there...by the method set forth in claim 1 or by the analyzing apparatus set forth in claim 11.
16. A manufacturing method for manufacturing a **liquid crystal display** device, comprising the steps of adhering a **TFT** substrate having an insulative transparent substrate provided with at least a **thin film transistor** and a **pixel electrode** to an opposing substrate having an insulative transparent substrate provided with at least an opposing electrode, at peripheries thereof with a prescribed gap therebetween, and injecting liquid crystal material into the gap, wherein a manufacturing process for **manufacturing** the **TFT substrate** and the opposing substrate include a cleaning step, a film forming step, an exposure step, an etching step, an ion implantation step and a heat...

31/TI,PD,PY,PN,K/2 (Item 2 from file: 348)

Positioning method and analysis method of fine foreign matter and analyzer used therefor.
Methode und Gerat zur Lagebestimmung und Analyse von feinem Fremdmaterial.
Methode et appareil pour determiner la position et analyser des particules contaminantes.
PATENT (CC, No, Kind, Date): EP 685731 A1 951206 (Basic)

15. The method of Claim 2, wherein the sample is an insulating transparent substrate in processing on which a **liquid crystal display** device is being formed.
16. The method of Claim 2, wherein the analyzer is a metallograph.
17. The method of Claim 2, wherein the analyzer...change in the beam light from the source of beam light caused by the foreign matter on the sample surface.
56. A method for manufacturing **liquid crystal display** devices comprising:
(a) adhering **TFT** substrate of a first insulating transparent substrate on which at least thin film transisters and **pixel electrodes** are provided, and a counter substrate of a second insulating transparent substrate on which counter electrodes are provided, on their circumference while keeping a specific...

...material in the clearance, the method further includes cleaning step, film forming step, exposure step, etching step, ion implantation step, and heat treatment step, for **manufacturing** the **TFT substrate** and the counter substrate,
at least one of the steps is accompanied by inspection substeps, at least one of the substeps is an analysis substep...the beam light at the position of the fine foreign matter, and
(8) analyzing content of the fine foreign matter.

57. A method for manufacturing **liquid crystal display** devices comprising:
(a) adhering **TFT** substrate of a first insulating transparent substrate on which at least thin film transisiters and **pixel electrodes** are provided, and a counter substrate of a second insulating transparent substrate on which counter electrodes are provided, on their circumference while keeping a specific...

...in the clearance, wherein the method further includes cleaning step, film forming step, exposure step, etching step, ion implantation step, and heat treatment step, for **manufacturing** the **TFT substrate** and the counter substrate, at least one of the steps being accompanied by inspection substeps, and at least one of said substeps is an analysis...

31/TI,PD,PY,PN,K/3 (Item 3 from file: 348)

Active matrix substrate
Substrat mit aktiver Matrix
Substrat a matrice active
PATENT (CC, No, Kind, Date): EP 603866 A1 940629 (Basic)
EP 603866 B1 020724

...ABSTRACT A1

An active-matrix substrate has a layered structure in which an upper region including a plurality of **pixel electrodes** (10) arranged in a matrix and a lower region including a plurality of thin film transistors (3) for driving the individual **pixel electrodes** are overlapped on each other. A planarization layer (11) is interposed between both the substrates. An active-matrix **liquid crystal display** device includes a main substrate (2) and a facing substrate (12) which are disposed to face to each other with a specified interval. A liquid crystal layer (13) having a specified thickness is held between both the substrates. A device bus line area including a plurality of **thin film transistor** devices and bus lines (7) is formed on the surface of the main substrate. A planarization layer (11) is formed to embed the irregularities on the surface of the device bus line area. **Pixel electrodes** in a matrix are formed on the flat surface of the planarization layer. An interval dimension between the adjacent **pixel electrodes** is set to be larger than a thickness dimension B of the liquid crystal layer, so that the subsidiary lateral electric field is made smaller...

...8. An active-matrix substrate as claimed in claim 7, wherein said planarization layer is formed on the light transmissive region.

9. An active-matrix **liquid crystal display** device comprising:
first and second substrates arranged in parallel to each other;
said first substrate comprising an upper region which has a plurality of **pixel electrodes** arranged in a matrix, a lower region which has a plurality of thin film transistors, each of which is associated with each **pixel electrode**, and a planarization layer arranged between the upper and lower regions to planarize a surface of the lower region; and

14. An active-matrix **liquid crystal display** device as claimed in claim 9, wherein said each **pixel electrode** has a symmetrical shape so that a lateral electric field caused between adjacent **pixel electrodes** in the vertical direction of the matrix is homogenized.

15. A method of **manufacturing** an active-matrix **substrate** comprising:
a first step of forming a first region which has a plurality of thin film transistors formed on a substrate;
a second step of...

16. A method as claimed in claim 15, wherein said second step comprises

the step of applying a liquid transparent region and then hardening the region.

17. A method as claimed in claim 15, further comprising a contacting step for electrically contacting the **pixel electrode** with the corresponding **thin film transistor** through a contact hole.

(1559),

a metal bus line pattern (1555) electrically connected to a source region (S) of each **thin film transistor** (1559) by way of a first contact hole (1554) through the layer insulating film (1553),

the black mask being comprised of a shading layer (1551) formed above each **thin film transistor** (1559) on the metal bus line pattern (1555) and the layer insulating film (1553),

the planarization layer (1556) being formed on the shading layer (1551) and the layer insulating film (1553),

2. An active-matrix **liquid crystal display** device, comprising:

first and second substrates arranged in parallel to each other,

the first substrate (1552) comprising an upper region which has a plurality of **pixel electrodes** (1558) arranged in a matrix, a lower region which has a plurality of thin film transistors (1559), each of which is associated to a corresponding **pixel electrode** (1559), and a planarization layer (1556) arranged between the upper and lower regions to planarize

a surface of the lower region,

a black mask formed at a boundary between adjacent **pixel electrodes** (1558

the black mask being comprised of a shading layer (1551) formed above each **thin film transistor** (1559) on the metal bus line pattern (1555) and the layer insulating film (1553),

the planarization layer (1556) being formed on the shading layer (1551) and the layer insulating film (1553),

the **pixel electrode** (1558) being electrically connected to a drain region (D) of the **thin film transistor** (1559) by way of a second hole (1557) passing through the planarization film (1556), the shading layer (1551) and the layer insulating film (1553).

the **pixel electrode** (1787) being electrically connected to a drain region (D) of the **thin film transistor** (1700) by way of a second hole (1785) passing through the planarization layer (1784) and the second layer insulating film (1781),

the black mask further comprising a shading layer (1786) covering the interior and the periphery of the second contact hole.

4. An active-matrix **liquid crystal display** device, comprising:

08/02/2002 09/808,957

31/TI,PD,PY,PN,K/4 (Item 4 from file: 349)

TFT ARRAY **SUBSTRATE**, METHOD OF **MANUFACTURE** THEREOF, AND **LCD** WITH **TFT** ARRAY SUBSTRATE
SUBSTRAT TABLEAU A MATRICE ACTIVE, PROCEDE DE FABRICATION, ET AFFICHEUR A CRISTAUX LIQUIDES MUNI D'UN SUBSTRAT TABLEAU A MATRICE ACTIVE
Patent and Priority Information (Country, Number, Date):
Patent: WO 200148547 A1 20010705 (WO 0148547)
Publication Year: 2001
A **TFT** array substrate including **pixel electrodes** (14') and TFTs (16) is manufactured using two or three photomasks. The **TFT** includes semiconductor silicon film deposited on an insulating substrate (1); gate oxide film (4') formed on channel regions of the silicon semiconductor film; a gate...

French Abstract
Selon l'invention, un substrat tableau a matrice active comprenant des **electrodes** de **pixels** (14') et des transistors a couches minces (**TFT**) (16) est fabrique au moyen de deux ou trois photomasques. Le **TFT** comprend une couche de silicium a semi-conducteurs pose sur un substrat isolant (1), une couche d'oxyde de grille (4') formee sur des regions...

34/TI,PD,PY,PN,K/1 (Item 1 from file: 348)

SHIFT REGISTER USED AS SELECTION LINE SCANNER FOR **LIQUID CRYSTAL DISPLAY**.
SHIFTREGISTER ZUM ABTASTEN DER ANSTEUERUNGSLEITUNGEN ZUR VERWENDUNG BEI EINER FLUSSIGKRISTALLANZEIGE.
REGISTRE A DECALAGE UTILISE COMME BALAYEUR DE LIGNES DE SELECTION POUR UN AFFICHEUR A CRISTAUX LIQUIDES.
PATENT (CC, No, Kind, Date): EP 586398 A1 940316 (Basic)
EP 586398 B1 951102
WO 9215992 920917

20, 21).

5. **Liquid crystal display** including a select line scanner circuit which selects the horizontal lines to be displayed and is **manufactured** on the same **substrate** as the liquid crystal cells, characterized in that this select line scanner includes a shift register according to any one of the preceding claims. ...

34/TI,PD,PY,PN,K/2 (Item 2 from file: 348)

Liquid crystal display panel.
Flussigkristall-Anzeigepaneel.
Panneau d'affichage a cristal liquide.
PATENT (CC, No, Kind, Date): EP 392840 A1 901017 (Basic)
EP 392840 B1 940309

.ABSTRACT A1
Molecules of the liquid crystal filled in the **liquid crystal display** panel are orientated along the rubbing directions of the upper and the lower substrates and the orientation thereof tends to be twisted in one direction...

...sufficiently rub the surfaces of the respective substrates since the substrates are provided with picture element electrodes thereon so that the surfaces are uneven. The **liquid crystal display** panel is heated to a transformation point so as to change into an isotropic phase after filling the liquid crystal, then is cooled rapidly, whereby there can be obtained a **liquid crystal display** panel in which the twisted directions of the orientation of the liquid crystal molecules are uniform. ...
(b) thereafter rapidly cooling the **liquid crystal display** panel at only one of said substrates (5) at a cooling rate higher than 1 (**degree**)**C/second** to cool substantially all of said **liquid crystal material** (1) down to an anisotropic temperature at which said liquid crystal material becomes anisotropic.
2. A method as set forth in claim 1, wherein said one of the **substrates** (5) is provided **with** a **thin film transistor** thereon and the other one of the substrates (3) with a color filter formed thereon.

...1, wherein step (b) includes cooling said liquid crystal material (1) at one of said substrates, after being heated in step (a), by pressing said **liquid crystal display** panel (11) **between first and** second members having heat conductivities different from each other.

08/02/2002 09/808,957

34/TI,PD,PY,PN,K/3 (Item 3 from file: 349)
DIALOG(R)File 349:(c) 2002 WIPO/Univentio. All rts. reserv.

A METHOD OF **MANUFACTURING** AN ACTIVE MATRIX **SUBSTRATE**
PROCEDE DE FABRICATION D'UN SUBSTRAT A MATRICE ACTIVE
Patent and Priority Information (Country, Number, Date):
Patent: WO 200256380 A1 20020718 (WO 0256380)
Publication Year: 2002

English Abstract
A method of **manufacturing** an active matrix **substrate** (1) comprising a row and column array of active elements (10) wherein each element (11) is associated with a **TFT** (13) having a gate electrode (306) connected to a corresponding row conductor (15) and source (320) and drain (321) electrodes connected to corresponding column conductors ...

1 . A method of **manufacturing** an active matrix **substrate** comprising
a row and column array of active elements wherein each element is associated
with a **thin film transistor** (**TFT**) having a gate electrode connected to a
corresponding row conductor and source and drain electrodes connected to corresponding column conductors; and ESID protective circuitry connected

12 An active matrix **substrate manufactured** by a method according
to any of the preceding claim.

13 An active matrix substrate comprising a row and column array of active elements wherein each element is associated with a **thin film transistor**
(**TFT**) having a gate electrode connected to a corresponding row conductor
and source and drain electrodes connected to corresponding column conductors; and ESID protective circuitry connected...

16 An active matrix **liquid crystal display** (AMLCD) comprising an
active matrix substrate according to any of claims 12 to 15.

34/TI,PD,PY,PN,K/4 (Item 4 from file: 349)

METHOD FOR **MANUFACTURING TFT** ARRAY **SUBSTRATE** OF **LIQUID CRYSTAL DISPLAY** DEVICE
PROCEDE DE FABRICATION DE SUBSTRAT A MATRICE ACTIVE D'AFFICHEUR A CRISTAUX LIQUIDES
Patent and Priority Information (Country, Number, Date):
Patent: WO 200208824 A1 20020131 (WO 0208824)
Publication Year: 2002

METHOD FOR **MANUFACTURING TFT** ARRAY **SUBSTRATE** OF **LIQUID CRYSTAL DISPLAY** DEVICE

34/TI,PD,PY,PN,K/5 (Item 5 from file: 349)

ELECTRIC CIRCUIT BOARD, **TFT** ARRAY SUBSTRATE USING THE SAME, AND **LIQUID CRYSTAL DISPLAY**
CARTE DE CIRCUIT ELECTRIQUE, SUBSTRAT A MATRICE **TFT** METTANT EN OEUVRE CETTE CARTE ET AFFICHAGE A CRISTAUX LIQUIDES
Patent and Priority Information (Country, Number, Date):
Patent: WO 200118774 A1 20010315 (WO 0118774)
Publication Year: 2001

ELECTRIC CIRCUIT BOARD, **TFT** ARRAY SUBSTRATE USING THE SAME, AND **LIQUID CRYSTAL DISPLAY**
CARTE DE CIRCUIT ELECTRIQUE, SUBSTRAT A MATRICE **TFT** METTANT EN OEUVRE CETTE CARTE ET AFFICHAGE A CRISTAUX LIQUIDES

English Abstract
A **TFT** array substrate used for a **liquid-crystal display** panel is disclosed of which the manufacturing process is simplified and the manufacturing cost is reduced by reducing the number of masks used in **manufacturing** the **TFT** array **substrate.**
A gate wiring metal film, a gate insulating film, a semiconductor film, and a contact electrode metal film are formed on a substrate surface. The ...

08/02/2002 09/808,957

34/TI,PD,PY,PN,K/6 (Item 6 from file: 349)

SUBSTRATE WITH CONDUCTOR FORMED OF LOW-RESISTANCE ALUMINUM ALLOY
SUBSTRAT A CONDUCTEUR EN ALLIAGE D'ALUMINIUM FAIBLE RESISTANCE
Patent and Priority Information (Country, Number, Date):
Patent: WO 9845881 A1 19981015
Publication Year: 1998

English Abstract
A wiring substrate is disclosed, which has optimal characteristics for, for example, an active matrix type **liquid crystal display** device with a **thin film transistor**. Wiring formed of an Al-Nd-Ti alloy thin film is formed on a glass substrate, and if necessary, a semiconductor element which is electrically...

Claim
... wherein the total concentration of the first and second metals contained in the aluminum alloy is 1.5 atm% or less.

16 A method of **manufacturing** a wiring **substrate**, comprising the steps of:
preparing a substrate;
forming on the substrate a conductor made of an aluminum alloy which contains at least neodymium and titanium in the aluminum alloy is 3.5 atm% or less.

37/TI,PD,PY,PN,K/1 (Item 1 from file: 348)

Electroluminescent display device
Elektroluminescenzanzeige
Dispositif d'affichage electroluminescent
PATENT (CC, No, Kind, Date): EP 1111574 A2 010627 (Basic)

...CLAIMS to claim 1, wherein said pair of source signal line driver circuits and said pair of gate signal line driver circuits are formed using a **TFT** on a substrate on which said pixel portion is also formed, and

wherein the driving frequency of said pair of source signal line driver circuits is 10 MHZ or more.

3. A device according to claim 1, wherein said EL element has a **pixel electrode**, an opposing **electrode**, and an EL layer interposed between said **pixel electrode** and said opposing **electrode**.

4. An EL display device wherein said device according to claim 1 is used.

5. A video camera wherein said device according to claim 1...
...lines connected to said second gate signal line driver circuit; and
a power supply line,
wherein said plurality of pixels each have a first switching **TFT**, a second switching **TFT**, a first eliminating **TFT**, a second eliminating **TFT**, a first EL driver **TFT**, a second driver **TFT**, and an EL element;

25. A device according to claim 12, wherein said EL element has a **pixel electrode**, an opposing **electrode**, and an EL layer interposed between said **pixel electrode** and said opposing **electrode**.

41. A method according to claim 38, wherein said an electric device has a **liquid crystal display** device having a response time of several ten microseconds or shorter.

45. A method according to claim 42, wherein said an electric device has a **liquid crystal display** device having a response time of several ten microseconds or shorter.

37/TI,PD,PY,PN,K/2 (Item 2 from file: 348)

Semiconductor device comprising organic resin and process for producing semiconductor device
Halbleiterbauelement mit organischem Harz und Prozess zur Herstellung des Bauelementes
Dispositif semiconducteur avec resine organique et son procede de fabrication
PATENT (CC, No, Kind, Date): EP 984492 A2 000308 (Basic)
EP 984492 A3 000517

..laser crystallization, since no difference in focal point of the laser light is formed among each position of the semiconductor film, crystallization can be uniformly **conducted**. Because the edge part of the gate wiring can be covered with the thick flattening film, implantation of an electron or a hole to the...

CLAIMS 1. A semiconductor device comprising:
a gate **electrode** formed on an insulating surface;
a gate insulating film comprising a flattening film comprising an insulating organic resin and an insulating inorganic film, formed to cover said gate **electrode**
4. A semiconductor device as claimed in claim 1, wherein said semiconductor device is one selected from a **liquid** crystal **display** device, an **electroluminescence display** device and an image sensor.
5. A semiconductor device comprising a circuit comprising a **thin film transistor** comprising:
a gate **electrode** formed on an insulating surface;
a gate insulating film formed on said gate **electrode**

...**claimed in claim 5, wherein**
a protective film comprising an insulating film is formed in contact with said semiconductor film, and
an impurity endowing a conductive type added to said source region and said drain region is added to at least a part of said protective film.
12. A semiconductor device as claimed in claim 5, wherein said circuit comprising said **thin film transistor** is a matrix circuit of an active matrix substrate, and a **pixel electrode** is connected to said **thin film transistor**.
13. A **liquid crystal display** device comprising said active matrix substrate claimed in claim 12.
14. An electronic apparatus comprising said **liquid crystal display** claimed in claim 13.
16. A semiconductor device as claimed in claim 5, wherein said semiconductor device is one selected from an **electroluminescence display** device and an image sensor.
17. A process for producing a semiconductor device comprising:
a step of forming a gate wiring on an insulating surface...

...rear projection display.
19. A process for producing a semiconductor device as claimed in claim

17, wherein said semiconductor device is one selected from a **liquid** crystal **display** device, an **electroluminescence display** device and an image sensor.

20. A process for producing a semiconductor device comprising a circuit comprising a **thin film transistor** formed on an insulating surface, said process comprising:

22. A process for producing a semiconductor device as claimed in claim 20, wherein said semiconductor device is one selected from a **liquid** crystal **display** device, an **electroluminescence display** device and an image sensor.

23. A process for producing a semiconductor device comprising a circuit comprising a **thin film transistor** formed on ... into an island form;

29. A semiconductor device as claimed in claim 23, wherein said semiconductor device is one selected from a **liquid** crystal **display** device, an **electroluminescence display** device and an image sensor.

39. A process for producing a semiconductor device as claimed in claim 35, wherein said semiconductor device is one selected from a **liquid** crystal **display** device, an **electroluminescence display** device and an image sensor.

40. A process for producing a semiconductor device as claimed in claim 17, wherein in said step of forming said...

...of at least from said step of forming said insulating inorganic film to said step of forming said semiconductor film having an amorphous component are **conducted** without exposing to the air, to successively accumulate said insulating inorganic film, said semiconductor film having an amorphous component, and said protective film.

41/TI,PD,PY,PN,K/1 (Item 1 from file: 348)

Active matrix **liquid-crystal display** device and method for making the same
Aktiv-Matrix-Flussigkristallanzeige und deren Herstellungsverfahren
Dispositif d'affichage a cristal liquide a matrice active et son procede de fabrication
PATENT (CC, No, Kind, Date): EP 919850 A2 990602 (Basic)
EP 919850 A3 000322

Disclosed is a method for making an active matrix **liquid-crystal display** device, this method having the steps of: forming interlayer insulating film, at least part of which composed of **organic** film, on a **TFT(thin-film transistor**) substrate with a structure where a **pixel electrode** and wiring are overlapped; patterning the **organic** film; and patterning a base layer using the patterned **organic** film as a mask. Also disclosed is an active matrix **liquid-crystal display** device, which has: a **TFT(thin-film transistor)** substrate with a structure where a **pixel electrode** and wiring are overlapped; and interlayer insulating film, at least part of which composed of **organic** film; wherein the **organic** film has a transmissivity of greater than 90% to g-line light and the heat resistance of **organic** film is higher than 250(degree)C.

CLAIMS 1. A method for making an active matrix **liquid-crystal display** device, comprising the steps of:
forming interlayer insulating film, at least part of which composed of **organic** film, on a **TFT(thin-film transistor)** substrate with a structure where a **pixel electrode** and wiring are overlapped;
patterning said **organic** film; and
patterning a base layer using the patterned **organic** film as a mask.
2. A method for making an active matrix **liquid-crystal display** device, according to claim 1, wherein
said **organic film** patterning step is **conducted** by wet etching, and said patterning of said base **layer** is **conducted** by dry etching using at least one kind of gas selected from O2)), CF4)), CHF3)) and SF6)).
3. A method for making an active matrix **liquid-crystal display** device, according to claim 2, further comprising the steps of:
forming **organic** film by applying resin and pre-baking it;
forming a resist pattern by applying resist on the surface of the formed **organic** film, and by baking, exposing and developing it;
forming a pattern of said **organic** film by wet-etching said **organic** film using said resist pattern as a mask;
dry-etching said base layer using said **organic** film pattern as a mask;
removing said resist; and
completely hardening said **organic** film pattern by re-baking.
4. A method for making an active matrix **liquid-crystal display** device, according to claim 3, wherein:

said resist is of positive-type resist using naphthoquinonediazo compound as a photosensitive agent, novolac resin as base resin and methylamine-system solvent or propyleneglycolmonoethyletheracetate solvent as a solvent,
said developing is **conducted** using tetramethylammoniumhydroxide (TMAH) solution, and
said removing of resist is **conducted** using a mixed solution of dimethylsulfoxide (DMSO) and monoethanolamine, ethyllactate or butyllactate.

5. A method for making an active matrix **liquid-crystal display** device, according to claim 4, wherein:
said **organic film** forming step is **conducted** by applying benzocyclobutene polymer using propyleneglycolmonoethyletheracetate as a solvent and pre-baking in the temperature range of 130 to 200(degree)C,
said **organic** film pattern forming step is **conducted** by wet-etching the **organic** film using a mixed solution of 1,3,5 triisopropylbenzene and aromatic system hydrocarbon or a mixed solution of glycolether and **synthetic** isoparaffin-system hydrocarbon, and
said **organic film** hardening step is **conducted** by re-baking in the temperature range of 240 to 300(degree)C.

6. A method for making an active matrix **liquid-crystal display** device, according to claim 4, wherein:

7. A method for making an active matrix **liquid-crystal display** device, according to claim 2, wherein:
said **organic** film pattern forming step is **conducted** so that the development of resist and the etching of **organic film** are simultaneously **conducted**.

8. A method for making an active matrix **liquid-crystal display** device, according to claim 7, further comprising the steps of:
forming **organic** film by applying resin and then pre-baking it;
applying resist on the surface of the formed **organic** film, baking, exposing it;
forming a pattern of said **organic** film by wet-etching said **organic** film simultaneously with forming a resist pattern by developing said resist;

41/TI,PD,PY,PN,K/2 (Item 2 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

Thin-film transistor with light-shielding film for use in liquid crystal devices, and method of making the same

Dunnschichttransistor mit lichtabschirmendem Film fur Flussigkristallvorrichtungen und Verfahren zu seiner Herstellung

Transistor a couche mince comportant une couche opaque pour utilisation dans des dispositifs a cristaux liquides et methode de sa fabrication

PATENT (CC, No, Kind, Date): EP 915365 A2 990512 (Basic)
EP 915365 A3 011017

A semiconductor device suitable for use in a flat display **LCD** according to an active matrix display type device comprising a-Si **thin film transistor** (**TFT**) elements is provided. The **TFT** which is a forward stagger type transistor is produced by forming a light shielding film (2) and, after forming a source **electrode** (5), a drain **electrode** and a drain signal line (6a), and a gate **electrode** (10) and a gate signal line (10a), the light shielding film (2) is removed except for the area covered by those **electrode** and signal lines. The number of manufacturing steps of this type of **TFT** is reduced by this manufacturing method which results in a reduction in the manufacturing cost. Furthermore, the **TFT** manufactured by this method is provided with a higher aperture which improves its operating performance.

CLAIMS 1. A semiconductor device of a forward stagger type **thin film transistor** element (**TFT**) which is arranged for each **pixel electrode** comprising:

a source **electrode** and a drain **electrode** formed on an insulating film formed on a surface of an insulating substrate;

an amorphous silicon (a-Si) film and a gate **electrode** formed on said insulating film in this order; and said drain **electrode** is connected to each **pixel electrode**;

wherein said insulating film possesses a light shielding property, and the light shielding insulating film on said substrate is removed from the surface of the substrate excluding an area covered by said source **electrode**, said drain **electrode** and said drain signal line, and said gate **electrode** and said gate signal line by using those **electrodes** and signal lines as a mask.

2. A semiconductor device according to claim 1, wherein said light shielding insulating film has a double layer structure formed by laminating an insulating **inorganic** film on the light shielding **organic** film.

3. A semiconductor device according to claim 1, wherein said semiconductor device is integrated in the a-SiTFT display device.

4. A semiconductor device according to claim 1, wherein said semiconductor device is integrated in a color **liquid crystal display** device operated by the a-SiTFT active matrix display system.

5. A color **liquid crystal display** device according to claim 4, wherein said area, where said insulating film of the semiconductor device is removed, is smoothened by a transparent smoothening film so as to yield a flat **liquid crystal**

display device.

6. A method of making a semiconductor device of a forward stagger type **thin film transistor** element (**TFT**) which is arranged for each **pixel electrode** comprising the steps of:

forming a source **electrode** and a drain **electrode** on an insulating film formed on a surface of the insulating substrate;

forming an amorphous silicon (a-Si) and a gate insulating film thereon on said insulating film so as to cover at least a part of said source and drain **electrodes**; and

connecting said drain **electrode** to each **pixel electrode**;

wherein said insulating film has a light shielding property, and the method further comprising;

removing said light shielding insulating film from the surface of the substrate excluding an area covered by said source **electrode**, said drain **electrode** and said drain signal line, and said gate **electrode** and said gate signal line by using those **electrodes** and signal lines as a mask.

7. A method of making the semiconductor device according to claim 6, wherein the method further comprising a step of

smoothening said area on said substrate, where said insulating film is removed, by a transparent smoothening film so as to yield a flat **liquid crystal display** device.

8. A liquid crystal flat display device according to claim 7, wherein said **liquid crystal display** device is an active matrix type display device, each **pixel electrode** of which is connected with the respective a-Si **TFT**, wherein said each **pixel electrode** is formed so as to overlap at least a part of either one of said drain signal line or said gate signal line, and said each **pixel electrode** is connected to said drain **electrode** through the contact hole formed through said transparent smoothening film.

41/TI,PD,PY,PN,K/3 (Item 3 from file: 348)

SEPARATING METHOD, METHOD FOR TRANSFERRING THIN FILM DEVICE, THIN FILM DEVICE, THIN FILM INTEGRATED CIRCUIT DEVICE, AND **LIQUID CRYSTAL DISPLAY** DEVICE MANUFACTUR
TRENNVERFAHREN, VERFAHREN ZUR UBERTRAGUNG EINES DUNNFILMBAUELEMENTS, DUNNFILMINTEGRIERTES SCHALTKREISBAUELEMENT UND UNTER VERWENDUNG DES UBERTRAGUNGSVERFAHRENS
METHODE DE SEPARATION, PROCEDE DE TRANSFERT D'UN DISPOSITIF A FILM MINCE, DISPOSITIF A FILM MINCE, DISPOSITIF A CIRCUIT INTEGRE A FILM MINCE ET DISPOSITIF D'AFF
PATENT (CC, No, Kind, Date): EP 858110 A1 980812 (Basic)
WO 9809333 980305

...CLAIMS film or a thin film device.
8. The exfoliating method according to any one of claims 3 to 6, wherein said transferred layer is a **thin film transistor**.
9. The exfoliating method according to any one of claims 3 to 8, wherein said transfer member is a transparent substrate.
10. The exfoliating method...

...is lower than 800 (degree)C.
12. The exfoliating method according to any one of claims 3 to 11, wherein said transfer member comprises a **synthetic** resin or glass.
13. The exfoliating method according to any one of claims 1 to 12, wherein said substrate has thermal resistance.
14. The exfoliating...

...said separation layer comprises a metal.
23. The exfoliating method according to any one of claims 1 to 18, wherein said separation layer comprises an **organic** polymer.
24. The exfoliating method according to claim 23, wherein said **organic** polymer has at least one adhere selected from the group consisting of -CH2))-, -CO-, -CONH-, -NH-, -COO-, -N=N-, and -CH=N-.
25. The exfoliating method according to either claim 23 or 24, wherein said **organic** polymer has an aromatic hydrocarbon group in the chemical formula.
wherein said transferred layer formed in said second step comprises a **thin film transistor**, and the thickness of said amorphous silicon layer formed in said first step is smaller than the thickness of the channel layer of said **thin film transistor** formed in said second step.
77. A **liquid crystal display** device comprising: a matrix of thin film transistors, a **pixel** section comprising **pixel electrodes** each connected to one end of each **thin film transistor**, and an active matrix substrate produced by transferring the thin film transistors in said pixel section by a method described in any one of claims...

44/TI,PD,PY,PN,K/1 (Item 1 from file: 348)

Liquid crystal display
Flussigkristallanzeige
Dispositif d'affichage a cristal liquide
PATENT (CC, No, Kind, Date): EP 1130455 A2 010905 (Basic)

A matrix-addressed type **liquid crystal display** apparatus having switching devices such as TFTs is provided, featuring that an increased effective voltage can be applied without causing hysteresis in V-T characteristics...

...which a display defect starts to appear, a high numerical aperture and a high contrast ratio have been achieved at the same time. In the **LCD** apparatus of the present invention, a gap between adjacent reverse tilt domains each formed in a portion of a pixel which is arranged corresponding to an arbitrary **pixel electrode** becomes broader than a minimum gap between adjacent **pixel electrodes** corresponding thereto, or a thickness of a liquid crystal cell in the portion between adjacent reverse tilt domains is set thinner than a thickness of...

1. A **liquid crystal display** apparatus having a liquid crystal cell comprising:
 a pair of substrates disposed so as to oppose to each other;
 a common **electrode** which is provided on one of said pair of substrates, and covered with a first orientation film;
 a plurality of **pixel electrodes** which are disposed in a matrix on the other of said pair of substrates, and covered with a second orientation film;
 a gap between adjacent reverse tilt domains each of which is formed in a portion of a pixel which is arranged corresponding to an arbitrary **pixel electrode** is arranged to become broader than a minimum gap between juxtaposed **pixel electrodes** thereof, or a thickness of a liquid crystal cell sandwiched in a portion between the adjacent reverse tilt domains inclusive thereof is arranged to become thinner than a thickness of a liquid crystal cell in a portion of the pixel.
2. The **liquid crystal display** apparatus according to claim 1, wherein a width of a **pixel electrode** corresponding to a longitudinal direction of the reverse tilt domain is set to become narrower than a width of a **pixel electrode** corresponding to a portion of the pixel in which no reverse tilt domain is formed.
3. The **liquid crystal display** apparatus according to claims 1 or 2, wherein the gap between the juxtaposed **pixel electrodes** is broadened partially in a direction orthogonal to a longitudinal direction of the reverse tilt domain.
4. The **liquid crystal display** apparatus according to claim 1, wherein said plurality of **pixel electrodes** are arranged in a staggered pattern like hound's tooth.
9. The **liquid crystal display** apparatus according to either one of claims 1-8, wherein a size of said **pixel electrode** is 5(mu)m2)-50(mu)m2).

10. A method of manufacturing the **liquid crystal display** apparatus as claimed in claim 1, wherein the method of **manufacturing** the **substrate** on the side of said switching devices comprises the steps of:

(a) forming a first interlayer-insulation layer on said substrate, forming a thin film Si layer thereon for forming a transistor, forming an oxide film on a surface thereof, constructing a **thin film transistor** by forming a gate **electrode** and a Cs **electrode** thereon, and further forming a second interlayer-insulation layer on the **thin film transistor;**

.pixel aperture, removing the third interlayer-insulation layer by etching from the portion of said contact hole, forming a second wiring layer thereon, forming an **organic** planar film on the whole surface thereof, then perforating a contact hole for a **pixel electrode** into the **organic** planar film, and forming a **pixel electrode** in such a pattern that a gap between adjacent reverse tilt domains each to be formed in a portion of a pixel arranged corresponding to an arbitrary **pixel electrode** becomes broader than a minimum gap between adjacent **pixel electrodes** thereof, and a step of, at the time of perforating the contact hole for the **pixel electrode** into the **organic** planar film, fabricating the **organic** planar film such that a thickness of the liquid crystal cell sandwiched in a portion between adjacent reverse tilt domains becomes thinner than a thickness of the liquid crystal cell in a portion of the pixel, and then forming the **pixel electrode**.

48/TI,PD,PY,PN,K/1 (Item 1 from file: 348)

SOLUTION FOR FORMING SILICA COATING FILM, PROCESS FOR PRODUCING THE SAME, AND SILICA COATING FILM AND PROCESS FOR PRODUCING THE SAME
LOSUNG FUR DIE HERSTELLUNG EINER SILICIUMOXIDBESCHICHTUNG, VERFAHREN ZUR HERSTELLUNG DIESER LOSUNG, SILICIUMOXIDBESCHICHTUNG UND VERFAHREN ZU SEINER HERSTELLUNG
SOLUTION POUR FORMER UN FILM DE REVETEMENT AU SILICE, PROCEDE DE PRODUCTION DE CETTE SOLUTION, ET FILM DE REVETEMENT AU SILICE ET SON PROCEDE DE PRODUCTION
PATENT (CC, No, Kind, Date): EP 1152044 A1 011107 (Basic)
WO 200026311 000511

...ABSTRACT coating film is applied to a surface of a substrate material in a dry atmosphere and the substrate material is put into an atmosphere containing **moisture**, a silica-based **coating** film excellent in terms of durability can be manufactured without adding a catalyst or carrying out heat treatment. In addition, by adding anhydrous silica fine ...

...CLAIMS siloxane bonds, and the chemical structure of the silica-based coating film does not contain hydrocarbon groups.
49. A passivation film for use in a **thin film transistor** array comprising a silica-based coating film wherein the silica-based coating film is formed on a surface of a substrate material by siloxane bonds...bonds, and the chemical structure of the silica-based coating film does not contain hydrocarbon groups.
51. (Amended) A passivation film for use in a **thin film transistor** array comprising a silica-based coating film wherein the silica-based coating film is formed on a surface of a substrate material by siloxane bonds passivation film for use in a **thin film transistor** array comprising the above-mentioned silica-based coating film.

08/02/2002 09/808,957

48/TI,PD,PY,PN,K/2 (Item 1 from file: 349)

RADIATION DETECTOR AND METHOD OF MANUFACTURE THEREOF
DETECTEUR DE RAYONNEMENT ET SON PROCEDE DE FABRICATION
Patent and Priority Information (Country, Number, Date):
Patent: WO 200175478 A1 20011011 (WO 0175478)
Publication Year: 2001

English Abstract
A semiconductor photoelectric film for X-ray detection formed on a **TFT** substrate is protected by a protective sheet or **film** to improve opaqueness, **moisture** resistance and weatherproofness so as to prevent or reduce changes of its performance with time. A radiation detector comprises a substrate (1) including a plurality...

48/TI,PD,PY,PN,K/3 (Item 2 from file: 349)

CORROSION RESISTANT IMAGER
DISPOSITIF D'IMAGERIE RESISTANT A LA CORROSION
Patent and Priority Information (Country, Number, Date):
Patent: WO 9832173 A1 19980723
Publication Year: 1998
pad according to claim 2, wherein said
first region further comprises a first layer of dielectric disposed over said gate contact region, a layer of **thin film transistor** (TIFT)
passivation layer overlaying said first dielectric layer and a diode
passivation layer overlaying said **TFT** passivation layer with both said
TIFT and diode passivation layers separating said first dielectric layer from said ITO conductor.

5 The contact pad according to...
...second
- 35
region further comprises an arrangement separating said source-drain contact region and said ITO conductor, said arrangement including:
(a) a layer of a **thin film transistor** (**TFT**)
passivation layer
disposed. over edge portions of said source-drain contact region in said second region so as to leave the central region of said source drain contact region at said second region free of said layer of **TFT**
0 passivation layer;
62 The photosensitive array of claim 58, wherein said
second tier inorganic barrier **layer** is a **moisture** barrier **layer**
comprising silicon nitride.

08/02/2002 09/808,957

52/TI,PD,PY,PN,K/1 (Item 1 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

Multilayer electrically conductive anti-reflective coating
Mehrschichtige elektrisch leitende antireflektierende Beschichtung
Revetement multicouche antireflechissant et electroconducteur
PATENT (CC, No, Kind, Date): EP 913712 A1 990506 (Basic)

...CLAIMS coating according to claim 1, having a bandwidth of more than about 1.60.

10. Anti-reflective coating according to claim 1, whereby the fifth **layer** has **moisture** barrier properties.
11. Anti-reflective coating according to claim 1, whereby the color of said coating is adjustable and reproducible.
12. A method for coating...

...coating for a polymer film which constitutes the front surface of a Cathode Ray Tube (CRT) used in television sets or computer monitors, or in **Liquid Crystal Displays** (**LC**

52/TI,PD,PY,PN,K/2 (Item 2 from file: 348)

PACKAGE FILM FOR EL PANEL, ITS MANUFACTURE, AND EL PANEL AND **LCD** MODULE EMPLOYING THE FILM
VERPACKUNGSFILM FUR ELEKTROLUMINESZENZPANEEL, VERFAHREN ZUR HERSTELLUNG, UND ELEKTROLUMINESZENZPANEEL UND FLUSSIGKRISTALL-ANZEIGEMODUL MIT DIESEM FILM
FILM D'EMBALLAGE POUR PANNEAU ELECTROLUMINESCENT, PROCEDE DE FABRICATION, ET PANNEAU ELECTROLUMINESCENT ET MODULE D'AFFICHAGE A CRISTAUX LIQUIDES UTILISANT CE F
PATENT (CC, No, Kind, Date): EP 891119 A1 990113 (Basic)
EP 891119 A1 990609
WO 9737516 971009

PACKAGE FILM FOR EL PANEL, ITS MANUFACTURE, AND EL PANEL AND **LCD** MODULE EMPLOYING THE FILM

...ABSTRACT A1
An EL panel package film comprises, for example, a PCTFE film or a PET **film** having a **moistureproof layer**. This EL panel package film has irregularities of 3 (mu)m or more in arithmetic average roughness (Ra) and 10 (mu)m or more in...
...polarity inversion of an alternate voltage applied to the EL panel are absorbed and dispersed by the irregularities formed on the package film surface. A **LCD** module has such an EL panel as the backlight. Noise from the **LCD** cell surface is reduced.

...CLAIMS on at least one of its surfaces.
6. The EL panel package film according to any one of claims 1 through 5, wherein the package **film** comprises a **moistureproof film**.
7. The EL panel package film according to claim 6, wherein the **moistureproof film** comprises polychlorotrifluoroethylene **film** or polyester **film** having a **moistureproof layer**.
8. A method for producing an EL panel package film, which comprises embossing at least one of surfaces of the EL panel package film with ...

...on the surface configuring at least the panel surface.
12. The EL panel according to any one of claims 9 through 11, wherein the package **film** comprises a **moistureproof film**.
13. The EL panel according to claim 12, wherein the **moistureproof film** comprises a polychlorotrifluoroethylene film or a polyester **film** having a **moistureproof layer**.
14. An **LCD** module, comprising the EL panel described in any one of claims 9 through 11.

52/TI,PD,PY,PN,K/3 (Item 3 from file: 348)

Transparent electro-conductive film, and AC powder type EL panel and **liquid crystal display** using the same.
Durchsichtiger elektrisch leitfahiger Film und elektrolumineszentes Paneel vom Wechselspannungstyp und dieses verwendende Flussigkristallanzeige.
Film transparent electroconducteur, et panneau electroluminescent a courant alternatif et affichage a cristal liquide l'utilisant.
PATENT (CC, No, Kind, Date): EP 390569 A2 901003 (Basic)
EP 390569 A3 901107
EP 390569 B1 931222

Transparent electro-conductive film, and AC powder type EL panel and **liquid crystal display** using the same.

...ABSTRACT permeation of the transparent electro-conductive film without any adverse effects on properties such as transparency. Also, a AC powder type EL panel and a **liquid crystal display** of the present invention have the above transparent electro-conductive films as a transparent electrode and a base thereof. Therefore, lower cost is achieved and...

...CLAIMS m.
10. The AC powder type EL panel according to claim 9 wherein said back electrode and said transparent electro-conductive film each have a **desiccant film** and **a moistureproof package film** laminated on the outer surface.
11. The AC powder type EL panel according to claim 9 wherein said hydrophobic resin particles are substantially spherical infusible...

...EL panel according to claim 9 wherein said emitting layer comprises an organic dielectric binder in which phosphor powder and organic fluorescent pigments are dispersed.
15. **A liquid crystal display**, comprising;
optical transparent polymer films,
a transparent electrode of a certain pattern shape including transparent electro-conductive thin films formed on one principal surface of...

...said polymer films contain 1 to 20% by weight of hydrophobic resin particles having an average particle diameter of 0.5 to 10 (mu)m.
16. **The liquid crystal display** according to claim 15 wherein said hydrophobic resin particles are substantially spherical infusible silicone resin particles.
17. **The liquid crystal display** according to claim 16 wherein said infusible silicone resin particles satisfy the condition that sphericity f shown in the following formula (I) is 0.8 ...

...wherein, A is a sectional area of the hydrophobic resin particles and D max is length of major axis of section of the hydrophobic resin **particles**.

18. **The liquid crystal display** according to claim 15 wherein said polymer films substantially comprise at least one selected from the group consisting of polyethersulfone, polyarylate and polyethylene terephthalate having...

08/02/2002 09/808,957

52/TI,PD,PY,PN,K/4 (Item 1 from file: 349)
DIALOG(R)File 349:(c) 2002 WIPO/Univentio. All rts. reserv.

OPTICAL MEASUREMENT DEVICE AND RELATED PROCESS
DISPOSITIF DE MESURE OPTIQUE ET PROCEDE CORRESPONDANT
Patent and Priority Information (Country, Number, Date):
Patent: WO 200141632 A2-A3 20010614 (WO 0141632)
Publication Year: 2001

Fulltext Availability:
Claims

Claim
... to transmit only tristimulus value bandwidths of the image to said image sensor. 105. The svstem of claim 104 wherein said display means is a **LCD**.
106. An instrument for acquiring a color image of a tooth comprising:
a handheld housing;
an image sensing device within said housing for sensing light...and accessible from outside said housing;
a window sealed within said sensing aperture-.
a display sealed within said display aperture.- and
said instrument beina substantially **moisture-proof** with the possible
exception of said at least one connection. whereby said instrument with the possible exception of said at least one connection can be...

52/TI,PD,PY,PN,K/5 (Item 2 from file: 349)

LIQUID CRYSTAL DISPLAY DEVICES USING A POLYMERIC SUPPORT LAYER
DISPOSITIFS AFFICHEURS A CRISTAUX LIQUIDES MUNIS D'UNE COUCHE DE SUPPORT POLYMERE
Patent and Priority Information (Country, Number, Date):
Patent: WO 9813722 A1 19980402
Publication Year: 1998

I A **liquid crystal display** device comprising a liquid crystal and one or more laminate structures, said laminate structure comprising a polarizer, a plastic support layer and a transparent cover...

...said transparent cover.

2 The device of claim I further comprising one or more layers selected from alignment layer, conducting layer, adhesive layer, anti-scratch **layer**, oxygen barrier **layer**, **moisture** barrier **layer**, diff-user layer, retardation layer and color filter.

3 The device of claim I operating in the transmissive mode.

4 The device of claim I...into a single layer.

29 The device of claim 1, wherein said cover material and said polarizer are combined into a single layer.

30 A **liquid crystal display** device comprising a liquid crystal and a first laminate structure and a second laminate structure, wherein said first laminate structure comprises a polarizer, a plastic...

52/TI,PD,PY,PN,K/6 (Item 3 from file: 349)

METHOD FOR COATING SEMICONDUCTOR ELEMENT WITH RESIN, COATING RESIN, AND **LIQUID CRYSTAL DISPLAY** DEVICE
PROCEDE DE REVETEMENT D'UN ELEMENT A SEMI-CONDUCTEUR D'UNE RESINE, RESINE DE REVETEMENT ET DISPOSITIF D'AFFICHAGE A CRISTAUX LIQUIDES
Patent and Priority Information (Country, Number, Date):
Patent: WO 9807065 A1 19980219
Publication Year: 1998

METHOD FOR COATING SEMICONDUCTOR ELEMENT WITH RESIN, COATING RESIN, AND **LIQUID CRYSTAL DISPLAY** DEVICE

English Abstract
...molded in a sheet-like state and the resin (14) is put around the element (2), and then, the element (2) and its periphery are **moisture**-proofed by **coating** them with the resin (14) and hardening the resin (14). Such a resin that is cured through a chemical reaction caused by heating, an ultraviolet...
? DS

58/TI,PD,PY,PN,K/1 (Item 1 from file: 348)

Semiconductor device comprising **organic** resin and process for producing semiconductor device
Halbleiterbauelement mit organischem Harz und Prozess zur Herstellung des Bauelementes
Dispositif semiconducteur avec resine organique et son procede de fabrication
PATENT (CC, No, Kind, Date): EP 984492 A2 000308 (Basic)
EP 984492 A3 000517

Semiconductor device comprising **organic** resin and process for producing semiconductor device

...ABSTRACT A2
In a **TFT** using a crystalline semiconductor film of a bottom gate type, a gate insulating film is flattened. On a substrate, an underlying film, a gate wiring and a gate insulating film are accumulated in this order. The gate insulating film comprises a flattening film comprising an insulating **organic** resin film, such as BCB, polyimide and acrylic, and an insulating **inorganic** film. Because the surface of the gate insulating film is flattened by the flattening film, a flat amorphous semiconductor film can be formed on the...

CLAIMS 1. A semiconductor device comprising:
a gate electrode formed on an insulating surface;
a gate insulating film comprising a flattening film comprising an insulating **organic** resin and an insulating **inorganic** film, formed to cover said gate electrode; and
a semiconductor layer covering said gate insulating film,

wherein said semiconductor layer comprises a crystalline semiconductor film...

...and a rear projection display.
4. A semiconductor device as claimed in claim 1, wherein said semiconductor device is one selected from a liquid crystal **display** device, an **electroluminescence display** device and an image sensor.
5. A semiconductor device comprising a circuit comprising a **thin film transistor** comprising:
a gate electrode formed on an insulating surface;
a gate insulating film formed on said gate electrode; and
a semiconductor layer, in which a...
12. A semiconductor device as claimed in claim 5, wherein said circuit comprising said **thin film transistor** is a matrix circuit of an active matrix substrate, and a **pixel electrode** is connected to said **thin film transistor**.
16. A semiconductor device as claimed in claim 5, wherein said semiconductor device is one selected from an **electroluminescence display** device and an image sens

19. A process for producing a semiconductor device as claimed in claim 17, wherein said semiconductor device is one selected from a liquid crystal **display** device, an **electroluminescence display** device and an image sensor.

20. A process for producing a semiconductor device comprising a circuit comprising a **thin film transistor** formed on an insulating surface, said process comprising:

a step of forming a gate wiring on an insulating surface;

a step of forming a flattening film comprising an insulating **organic** resin to cover said gate wiring;

60/TI,PD,PY,PN,K/1 (Item 1 from file: 348)

Liquid crystal display
Flussigkristallanzeige
Dispositif d'affichage a cristal liquide
PATENT (CC, No, Kind, Date): EP 1130455 A2 010905 (Basic)

...ABSTRACT the present invention, a gap between adjacent reverse tilt domains each formed in a portion of a pixel which is arranged corresponding to an arbitrary **pixel electrode** becomes broader than a minimum gap between adjacent **pixel electrodes** corresponding thereto, or a thickness of a liquid crystal cell in the portion between adjacent reverse tilt domains is set thinner than a thickness of...

...CLAIMS A liquid crystal display apparatus having a liquid crystal cell comprising:
a pair of substrates disposed so as to oppose to each other;
a common **electrode** which is provided on one of said pair of substrates, and covered with a first orientation film;
a plurality of **pixel electrodes** which are disposed in a matrix on the other of said pair of substrates, and covered with a second orientation film;
a switching device connected to each **pixel electrode**; and
a liquid crystal which is sealed between said first and second orientation films on said pair of substrates, wherein
2. The liquid crystal display apparatus according to claim 1, wherein a width of a **pixel electrode** corresponding to a longitudinal direction of the reverse tilt domain is set to become narrower than a width of a **pixel electrode** corresponding to a portion of the pixel in which no reverse tilt domain is formed.
3. The liquid crystal display apparatus according to claims 1 or 2, wherein the gap between the juxtaposed **pixel electrodes** is broadened partially in a direction orthogonal to a longitudinal direction of the reverse tilt domain.
steps of:
(a) forming a first interlayer-insulation layer on said substrate, forming a thin film Si layer thereon for forming a transistor, forming an oxide film on a surface thereof, constructing a **thin film transistor** by forming a gate **electrode** and a Cs **electrode** thereon, and further forming a second interlayer-insulation layer on the **thin film transistor**;

...pixel aperture, removing the third interlayer-insulation layer by etching from the portion of said contact hole, forming a second wiring layer thereon, forming an **organic** planar film on the whole surface thereof, then perforating a contact hole for a **pixel electrode** into the **organic** planar film, and forming a **pixel electrode** in such a pattern that a gap between adjacent reverse tilt domains each to be formed in a portion of a pixel arranged corresponding to an arbitrary **pixel electrode** becomes broader than a minimum gap between adjacent

pixel electrodes thereof, and a step of, at the time of perforating the contact hole for the **pixel electrode** into the **organic** planar film, fabricating the **organic** planar film such that a thickness of the liquid crystal cell sandwiched in a portion between adjacent reverse tilt domains becomes thinner than a thickness of the liquid crystal cell in a portion of the pixel, and then forming the **pixel electrode**.

60/TI,PD,PY,PN,K/2 (Item 2 from file: 348)

Planar x-ray detector
Rontgenstrahl-Flachendetektor
Detecteur plat de rayons X
PATENT (CC, No, Kind, Date): EP 1120833 A2 010801 (Basic)

...ABSTRACT A2

A planar X-ray detector has an X-ray charge conversion film (403) converting an incident X-ray into electric charges, **pixel electrodes** (503) provided on the X-ray charge conversion film (403) corresponding to respective pixels arranged in an array, switching elements (402) connected to the respective **pixel electrodes** (503), signal lines (408), each of which is connected to a column of switching elements (402), scanning lines (407), each of which transmits driving signals to a raw of switching elements (402), and a common **electrode** (603) provided on the surface of the X-ray charge conversion film (403) opposite to the surface on which the **pixel electrodes** (503) are provided. The X-ray charge conversion film contains an X-ray sensitive material (110) made of **inorganic** semiconductor particles, and a carrier transport material (109) made of an **organic** semiconductor.

1. A planar X-ray detector, characterized by comprising:
   an X-ray charge conversion film (403) converting an incident X-ray into electric charges;
   pixel electrodes (503) provided on the X-ray charge conversion film (403) corresponding to respective pixels arranged in an array;
   switching elements (402) connected to the respective **pixel electrodes** (503);
   signal lines (408), each of which is connected to a column of switching elements (402);
   scanning lines (407), each of which transmits driving signals to a raw of switching elements (402) ; and
   a common **electrode** (603) provided on the surface of the X-ray charge conversion film (403) opposite to the surface on which the **pixel electrodes** (503) are provided;
   wherein the X-ray charge conversion film (403) contains an X-ray sensitive material (110) comprising **inorganic** semiconductor particles, and a carrier transport material (109) comprising an **organic** semiconductor.
2. The planar X-ray detector according to claim 1, characterized in that the X-ray sensitive material (110) is made of at least...

...or less.

6. The planar X-ray detector according to any of claims 1 to 5, characterized in that the X-ray sensitive material contains **inorganic** semiconductor particles (110) having a relatively large particle size and **inorganic** semiconductor particles (110a) having a relatively small particle size.
7. The planar X-ray detector according to any of claims 1 to 6, characterized in...

...density of the X-ray sensitive material (110) in the X-ray charge

conversion film (403) is relatively high on the side of the common **electrode** (603) and is relatively low on the side of the **pixel electrodes** (503).

21. The planar X-ray detector according to any of claims 15 to 20, characterized by further comprising a hole transport layer (108) disposed between the X-ray charge conversion film (403) and one of the **electrodes** (503), and an electron transport layer (111) disposed between the X-ray charge conversion film (403) and the other one of the **electrodes** (603)

60/TI,PD,PY,PN,K/3 (Item 3 from file: 348)

Method of fabricating and structure of an active matrix light-emitting display device
Herstellungsverfahren und Struktur einer Licht emittierenden Anzeigevorrichtung mit aktiver Matrix
Methode de fabrication et structure d'un dispositif d'affichage emetteur de lumiere a matrice active
PATENT (CC, No, Kind, Date): EP 996176 A1 000426 (Basic)

...ABSTRACT A1

The invention concerns active matrix light-emitting display devices and a method of their fabrication wherein the problem of chemically unstable cathode **electrode** layers is solved, simultaneously offering a considerably higher aperture ratio and brightness with rather low driving voltages. These advantages are achieved by separate **manufacture** of a first **substrate** bearing **TFT** elements of which the source and drain regions are at first covered by a non-**conductive** passivation **layer** followed by a deposition of a chemically stable cathode material layer and deposition of an appropriately selected EL material layer. The anode side substrate is independently prepared by at first depositing an anode layer followed by application of an EL layer, then the two independently **manufactured** layered **substrates** are alligned face-to-face and are combined to a unified structure under application of heat and pressure, the temperature being selected to have the...

CLAIMS 1. A method for fabricating an active matrix display device formed of a plurality of pixels and comprising:
- at least one **thin film transistor** element (**TFT** element) (2) is deposited on a first substrate (1) for each pixel,
- at least the source region (S) and the channel region (C) of said at least one **TFT** element (2) for each pixel are covered by a non-**conductive** passivation **layer** (3) such as to leave parts or all of the drain region (D) uncovered,
- a cathode material layer structured into a plurality of **pixel electrode** regions (5a, 5b, ...) is deposited so as to cover at least a substantial part of each of said **TFT** elements,

10. An active matrix display device formed of a plurality of pixels and comprising:
- at least one **thin film transistor** (**TFT**) element adhered on a first substrate (1) for each **pixel**;
- a structured non-**conductive** passivation **layer** (3) covering the source (S) and drain (D) regions of said **TFT** element (2) and leaving at least part of the drain region (D) uncovered;
- a low work function material layer structured into **pixel electrode** areas (5a, 5b, ...) and electrically contacting said uncovered part of said drain regions;
- a second substrate (2) bearing an electrically **conducting**

high work function **layer** (7a, 7b, ...); and
- an active **organic** or polymeric electroluminescent EL material layer (6, 6') placed between said low work function pixel structured layer and said high work function layer on said...

...carboxylic acids, hydroxamine, thiols, phosphonates, sulfonates and/or amines.

13. The display device according to claim 11, characterized in that molecules attached to said modified **electrodes** comprise the same functional group for light emission and/or charge transport as the active **organic** or polymeric layer in the device adjacent to said modified **electrode**.

60/TI,PD,PY,PN,K/4 (Item 4 from file: 348)

Semiconductor device comprising **organic** resin and process for producing semiconductor device
Halbleiterbauelement mit organischem Harz und Prozess zur Herstellung des Bauelementes
Dispositif semiconducteur avec resine organique et son procede de fabrication
PATENT (CC, No, Kind, Date): EP 984492 A2 000308 (Basic)
EP 984492 A3 000517

CLAIMS 1. A semiconductor device comprising:
a gate **electrode** formed on an insulating surface;
a gate insulating film comprising a flattening film comprising an insulating **organic** resin and an insulating **inorganic** film, formed to cover said gate **electrode**; and
a semiconductor layer covering said gate insulating film,

wherein said semiconductor layer comprises a crystalline semiconductor film.
2. A semiconductor device as claimed in...

...one selected from a liquid crystal display device, an electroluminescence display device and an image sensor.
5. A semiconductor device comprising a circuit comprising a **thin film transistor** comprising:
a gate **electrode** formed on an insulating surface;
a gate insulating film formed on said gate **electrode**; and
a semiconductor layer, in which a channel forming region, a source region and a drain region are formed, formed on said gate insulating film...
a protective film comprising an insulating film is formed in contact with said semiconductor film, and
an impurity endowing a **conductive** type added to said source region and said drain region is added to at least a part of said protective film.
10. A semiconductor device...

...a direction of a channel length larger than said channel length.
12. A semiconductor device as claimed in claim 5, wherein said circuit comprising said **thin film transistor** is a matrix circuit of an active matrix substrate, and a **pixel electrode** is connected to said **thin film transistor**.
a step of forming a flattening film comprising an insulating **organic** resin to cover said gate wiring;
a step of forming an insulating **inorganic** film in contact with said flattening film;
a step of forming a semiconductor film having an amorphous component to cover said insulating **inorganic** film

60/TI,PD,PY,PN,K/5 (Item 5 from file: 348)

Active matrix liquid-crystal display device and method for making the same
Aktiv-Matrix-Flussigkristallanzeige und deren Herstellungsverfahren
Dispositif d'affichage a cristal liquide a matrice active et son procede de fabrication
PATENT (CC, No, Kind, Date): EP 919850 A2 990602 (Basic)
EP 919850 A3 000322

...ABSTRACT making an active matrix liquid-crystal display device, this method having the steps of: forming interlayer insulating film, at least part of which composed of **organic** film, on a **TFT(thin-film transistor)** substrate with a structure where a **pixel electrode** and wiring are overlapped; patterning the **organic** film; and patterning a base layer using the patterned **organic** film as a mask. Also disclosed is an active matrix liquid-crystal display device, which has: a **TFT(thin-film transistor)** substrate with a structure where a **pixel electrode** and wiring are overlapped; and interlayer insulating film, at least part of which composed of **organic** film; wherein the **organic** film has a transmissivity of greater than 90% to g-line light and the heat resistance of **organic** film is higher than 250(degree)C.

...CLAIMS method for making an active matrix liquid-crystal display device, comprising the steps of:
forming interlayer insulating film, at least part of which composed of **organic** film, on a **TFT(thin-film transistor)** substrate with a structure where a **pixel electrode** and wiring are overlapped;
patterning said **organic** film; and
patterning a base layer using the patterned **organic** film as a mask.
2. A method for making an active matrix liquid-crystal display device, according to claim 1, wherein
said **organic film** patterning step is **conducted** by wet etching, and said patterning of said base **layer** is **conducted** by dry etching using at least one kind of gas selected from O2)), CF4)), CHF3)) and SF6)).
said **organic** film pattern forming step is **conducted** by wet-etching the **organic** film using a mixed solution of 1,3,5 triisopropylbenzene and aromatic system hydrocarbon or a mixed solution of glycolether and **synthetic** isoparaffin-system hydrocarbon, and
said **organic film** hardening step is **conducted** by re-baking in the temperature range of 240 to 300(degree)C.
6. A method for making an active mat
wet-etching the **organic** film using a buffered hydrofluoric acid solution, and
said **organic film** hardening step is **conducted** by re-baking in the temperature range of 240 to 300(degree)C.
7. A method for making an active matrix liquid-crystal display device, according to claim 2, wherein:

re-baking in the temperature range of 230 to 280(degree)C.

20. An active matrix liquid-crystal display device, comprising:
a **TFT**(**thin-film transistor**) substrate with a structure where a **pixel electrode** and wiring are overlapped; and
interlayer insulating film, at least part of which composed of **organic** fil

25. An active matrix liquid-crystal display device, according to claim 20, wherein said interlayer insulating **film** is formed by **conducting** the steps of:
patterning said **organic** film composing at least part of said interlayer insulating film;

60/TI,PD,PY,PN,K/6 (Item 6 from file: 348)

ACTIVE MATRIX DISPLAY
ANZEIGEVORRICHTUNG MIT AKTIVER MATRIX
AFFICHEUR A MATRICE ACTIVE
PATENT (CC, No, Kind, Date): EP 940797 A1 990908 (Basic)
WO 9910862 990304

...CLAIMS a matrix delimited by the data lines and the scanning lines; each of the pixels being provided with a thin film luminescent device having a **conduction** control circuit containing a **thin film transistor** for supplying a scanning signal to a gate **electrode** through one of the scanning lines, a **pixel electrode**, an **organic** semiconductive film deposited above the **pixel electrode**, and an opposite **electrode** deposited above the **organic** semiconductive film; the thin film luminescent device emitting light based on an image signal supplied from the data line through the **conduction** control circuit; wherein

the region for forming the **organic** semiconductive film is divided by an insulating film which is thicker than the **organic** semiconductive film; and

the insulating film comprises a lower insulating layer which is formed of an **inorganic** material and is thicker than the **organic** semiconductive film, and an upper insulating layer which is deposited on the lower insulating layer and is formed of an **organic** material.

..a matrix delimited by the data lines and the scanning lines; each of the pixels being provided with a thin film luminescent device having a **conduction** control circuit containing a **thin film transistor** for supplying a scanning signal to a gate **electrode** through one of the scanning lines, a **pixel electrode**, an **organic** semiconductive film deposited above the **pixel electrode**, and an opposite **electrode** deposited above the **organic** semiconductive film; the thin film luminescent device emitting light based on an image signal supplied from the data line through the **conduction** control circuit; wherein

the region for forming the **organic** semiconductive film is divided by an insulating film which is thicker than the **organic** semiconductive film; and

the insulating film comprises a lower insulating layer composed of an **inorganic** material, and an upper insulating layer, composed of an **inorganic** material, so as to have a width which is narrower than that of the lower insulating layer.

4. An active matrix display device according to any one of claims 1 to 3, wherein the **conduction** control circuit is provided with a first **TFT** for supplying the scanning signal to the gate **electrode** and a second **TFT** of which the gate **electrode** is connected to the data line through the first **TF**

7. An active matrix display device according to any one of claims 1 to 6,

wherein a region overlapping the area for forming the conduction control circuit in the region for forming the **pixel electrode** is covered with the insulating film.

..of claims 1 to 4, wherein the lower insulating layer of the insulating film is formed so as to cover the area for forming the **conduction** control circuit in the region for forming the **pixel electrode**, the data line, the common feed line, and the scanning line, whereas the upper insulating layer is formed so as to form a striped pattern along the data line; and the **organic** semiconductive film is formed in the region delimited by the striped pattern of the upper insulating layer.

10. An active matrix display device according to...

...An active matrix display device according to any one of claims 1 to 11, wherein the insulating film has first discontinuities portion so that opposite **electrodes** of adjacent **pixels** are connected to each other at flat sections formed by the first discontinuities portion.

60/TI,PD,PY,PN,K/7 (Item 7 from file: 348)

ACTIVE MATRIX DISPLAY
ANZEIGEVORRICHTUNG MIT AKTIVER MATRIX
DISPOSITIF D'AFFICHAGE A MATRICE ACTIVE
PATENT (CC, No, Kind, Date): EP 940796 A1 990908 (Basic)
WO 9910861 990304

...ABSTRACT order to provide an active matrix display device in which parasitic capacitance or the like is suppressed by forming a thick insulating film around an **organic** semiconductor film and disconnection or the like does not occur in the opposing **electrode** formed on the upper layer of the thick insulating film, in an active matrix display device (1), first, a bank layer (bank) composed of a resist film is formed along data lines (sig) and scanning lines (gate), and by depositing an opposing **electrode** (op) of a thin film luminescent element (40) on the upper layer side of the bank layer (bank), capacitance that parasitizes the data lines

...CLAIMS in a matrix by the data lines and the scanning lines; each of the pixels being provided with a thin film luminescent element comprising a **conduction** control circuit having a **thin film transistor** for supplying scanning signals to a gate **electrode** through the scanning lines, a **pixel electrode**, an **organic** semiconductor film deposited above the **pixel electrode**, and an opposing **electrode** formed at least over the entire surface of the display area above the **organic** semiconductor film; the thin film luminescent element emitting light in response to picture signals supplied from the data lines through the **conduction** control circuit;

wherein a region for forming the **organic** semiconductor film is delimited by an insulating film which is thicker than the **organic** semiconductor film and formed below the opposing **electrode**; and

the insulating film is provided with a discontinuities portion for connecting the individual opposing **electrode** sections of the **pixels** to each other through a planar section not having a step formed by the insulating film.

2. An active matrix display device according to Claim 1, wherein the **conduction** control circuit comprises a first **thin film transistor** in which the scanning signals are supplied toa gate **electrode** and a second **thin film transistor** in which a gate **electrode** is connected to the data lines through the first **thin film transistor**; and

the second **thin film transistor** and the thin film luminescent element are connected in series between a common feeder formed independently of the data lines and the scanning lines for feeding a driving current and the opposing **electrode**

9. An active matrix display device according to any one of Claims 5 to 8, wherein, in the region in which the **pixel electrode** is

formed, a region overlapping the region in which the **conduction** control circuit is formed is covered with the insulating film.

60/TI,PD,PY,PN,K/8 (Item 8 from file: 348)

Thin-film transistor with light-shielding film for use in liquid crystal devices, and method of making the same

Dunnschichttransistor mit lichtabschirmendem Film fur Flussigkristallvorrichtungen und Verfahren zu seiner Herstellung

Transistor a couche mince comportant une couche opaque pour utilisation dans des dispositifs a cristaux liquides et methode de sa fabrication

PATENT (CC, No, Kind, Date): EP 915365 A2 990512 (Basic)
EP 915365 A3 011017

A semiconductor device suitable for use in a flat display LCD according to an active matrix display type device comprising a-Si **thin film transistor** (**TFT**) elements is provided. The **TFT** which is a forward stagger type transistor is produced by forming a light shielding film (2) and, after forming a source **electrode** (5), a drain **electrode** and a drain signal line (6a), and a gate **electrode** (10) and a gate signal line (10a), the light shielding film (2) is removed except for the area covered by those **electrode** and signal lines. The number of manufacturing steps of this type of **TFT** is reduced by this manufacturing method which results in a reduction in the manufacturing cost. Furthermore, the **TFT** manufactured by this method is provided with a higher aperture which improves its operating performance.

CLAIMS 1. A semiconductor device of a forward stagger type **thin film transistor** element (**TFT**) which is arranged for each **pixel electrode** comprising:

a source **electrode** and a drain **electrode** formed on an insulating film formed on a surface of an insulating substrate;

an amorphous silicon (a-Si) film and a gate **electrode** formed on said insulating film in this order; and said drain **electrode** is connected to each **pixel electrode**;

wherein said insulating film possesses a light shielding property, and the light shielding insulating film on said substrate is removed from the surface of the substrate excluding an area covered by said source **electrode**, said drain **electrode** and said drain signal line, and said gate **electrode** and said gate signal line by using those **electrodes** and signal lines as a mask.

2. A semiconductor device according to claim 1, wherein said light shielding insulating film has a double layer structure formed by laminating an insulating **inorganic** film on the light shielding **organic** film.

6. A method of making a semiconductor device of a forward stagger type **thin film transistor** element (**TFT**) which is arranged for each **pixel electrode** comprising the steps of:

forming a source **electrode** and a drain **electrode** on an insulating film formed on a surface of the insulating substrate;

forming an amorphous silicon (a-Si) and a gate insulating film thereon on said insulating film so as to cover at least a part of said source

and drain **electrodes**

...8. A liquid crystal flat display device according to claim 7, wherein said liquid crystal display device is an active matrix type display device, each **pixel electrode** of which is connected with the respective a-Si **TFT**, wherein said each **pixel electrode** is formed so as to overlap at least a part of either one of said drain signal line or said gate signal line, and said each **pixel electrode** is connected to said drain **electrode** through the contact hole formed through said transparent smoothening film.

60/TI,PD,PY,PN,K/10 (Item 10 from file: 349)

THIN-FILM TRANSISTOR CIRCUITRY
CIRCUIT DE TRANSISTOR A FILM MINCE A SENSIBILITE REDUITE AUX VARIATIONS DE LA TENSION DE SEUIL DU TRANSISTOR
Patent and Priority Information (Country, Number, Date):
Patent: WO 200148822 A2-A3 20010705 (WO 0148822)
Publication Year: 2001

A circuit design technique polysilicon **thin-film transistor** (**TFT**) circuitry produces circuits that are relatively less sensitive to threshold variations among the **TFT**'s than circuits designed using conventional techniques. The circuit is designed such that thin-film transistors that are sensititve to threshold variations are made larger...

...may be used with any display technology that uses an active matrix and stores image data on a capacitance in the pixel, including without limitation, **organic** light emitting diodes, electroluminescent devices, and **inorganic** light emitting diodes.

2 A method according to claim 1, wherein each of the **TFT**'s in the layout has a length to width ratio and the step of increasing the identified **TFT**'s in size preserves the length to width ratio of the identified **TFT**'s.

3 . A pixel structure for an active matrix display comprising:
a drive transistor having a principal **conduction** path coupled between a
source of operational power and an active pixel element, the drive transistor having a
control **electrode**;
a select transistor having a principal **conductive** path between a data line and the control **electrode** of the drive transistor, and having a further control **electrode**
coupled to a select line;
wherein the control **electrode** of the drive transistor exhibits sufficient capacitance to the select transistor to store a control value received from the data line via the select transistor...

7 A pixel structure according to claim 6 wherein the control **electrode**
of the drive transistor forms a capacitance with the principal **conductive** path of the drive transistor when the drive transistor **conducts** current and forms a capacitance with a further **electrode** coupled to a predetermined electric potential when the drive transistor is not **conducting** current.

8 A **pixel** structure for an active matrix display having thin-film transistors (**TFT**'s) implemented in polysilicon comprising:
an active pixel element,

a drive **TFT** having a source **electrode** coupled to a source of operational
power and a drain **electrode** coupled to the active pixel element, the drive **TFT** having a
gate **electrode** and exhibiting a gate to source threshold potential;
a select **TFT** having a principal **conductive** path between a data line and the control **electrode** of the drive **TFT**, and
having a further control **electrode** coupled to a select line; and
a capacitor, coupled between the control **electrode** of the drive transistor
I I and the source of operational power;
9 A pixel structure according to claim 8, wherein the drive **TFT** is designed with a length to width ratio which produces a predetermined current response characteristic.
I 10. A pixel structure according to claim 9, wherein the active pixel element is an **organic** light emitting diode (OLED) device.

60/TI,PD,PY,PN,K/11 (Item 11 from file: 349)

APPARATUSES AND METHODS FOR FORMING ASSEMBLIES
APPAREILS ET PROCEDES DE FORMATION D'ENSEMBLES
Patent and Priority Information (Country, Number, Date):
Patent: WO 200046854 A1 20000810 (WO 0046854)
Publication Year: 2000

8 The flexible display device as in claim I wherein said active matrix backplane comprises at least one **electrode** for each picture element.

10 The flexible display device...
...method of manufacturing a flexible active matrix display panel comprising:
depositing a plurality of shaped blocks onto a flexible substrate, each said
block has a **pixel electrode** thereon; and
coupling electrically said plurality of blocks to form an active matrix backplane.

19 The method as in claim I I wherein the flexible active matrix display panel comprises an **organic** light emitting diode.

20 The method as in claim I I wherein the flexible active matrix display panel comprises an **inorganic** light emitting diode.

39 The method as in claim 31 wherein the flexible passive matrix display panel comprises an **organic** light emitting diode.

40 The method as in claim 31 wherein the flexible active matrix display panel comprises an **inorganic** light emitting diode.

62/TI,PD,PY,PN,K/1 (Item 1 from file: 348)

Semiconductor device comprising organic resin and process for producing semiconductor device
Halbleiterbauelement mit organischem Harz und Prozess zur Herstellung des Bauelementes
Dispositif semiconducteur avec resine organique et son procede de fabrication
PATENT (CC, No, Kind, Date): EP 984492 A2 000308 (Basic)
EP 984492 A3 000517

...ABSTRACT A2
In a **TFT** using a crystalline semiconductor film of a bottom gate type, a gate insulating film is flattened. On a substrate, an underlying film, a gate wiring...

...this order. The gate insulating film comprises a flatten... ...m comprising an insulating organic resin film, such as BCB, po... ...ide and acrylic, and an insulating **inorganic** film. Because the surface of the gate insulating film is flattened by the flattening film, a flat amorphous semiconductor film can be formed on the...

4. A semiconductor device as claimed in claim 1, wherein said semiconductor device is one selected from a **liquid** crystal **display** device, an **electroluminescence display** device and an image sensor.
5. A semiconductor device comprising a circuit comprising a **thin film transistor** comprising:
a gate electrode formed on an insulating surface;
a gate insulating film formed on said gate electrode; and
a semiconductor layer, in which a...
...on which said semiconductor layer is provided, a flattening film comprising an insulating organic resin formed in contact with said gate electrode, and an insulating **inorganic** film accumulated thereto.
6. A semiconductor device as claimed in claim 5, wherein said flattening film comprises a material selected from benzocyclobutene, polyimide and acrylic...

...a direction of a channel length larger than said channel length.
12. A semiconductor device as claimed in claim 5, wherein said circuit comprising said **thin film transistor** is a matrix circuit of an active matrix substrate, and a pixel electrode is connected to said **thin film transistor**.
13. A **liquid crystal display** device comprising said active matrix substrate claimed in claim 12.
14. An electronic apparatus comprising said **liquid crystal display** claimed in claim 13.
15. A semiconductor device as claimed in claim 5, wherein said semiconductor device is incorporated into a product selected from a ...
a step of forming a semiconductor film having an amorphous component to cover said insulating **inorganic** film; and

a step of crystallizing said semiconductor film having an amorphous component to form a crystalline semiconductor film.

18. A process for producing a...

...rear projection display.

19. A process for producing a semiconductor device as claimed in claim 17, wherein said semiconductor device is one selected from a **liquid** crystal **display** device, an **electroluminescence display** device and an image sensor.

20. A process for producing a semiconductor device comprising a circuit comprising a **thin film transistor** formed on an insulating surface, said process comprising:

22. A process for producing a semiconductor device as claimed in claim 20, wherein said semiconductor device is one selected from a **liquid** crystal **display** device, an **electroluminescence display** device and an image sensor.

23. A process for producing a semiconductor device comprising a circuit comprising a **thin film transistor** formed on ... insulating surface;

a step of forming a flattening film comprising an insulating organic resin to cover said gate wiring;

a step of forming an insulating **inorganic** film in contact with said flattening film;

a step of forming a semiconductor film having an amorphous component to cover said insulating **inorganic** film;

39. A process for producing a semiconductor device as claimed in claim 35, wherein said semiconductor device is one selected from a **liquid** crystal **display** device, an **electroluminescence display** device and an image sensor.